

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE
Multiband UWB Transceivers

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Abstract

This paper presents the design of UWB transceivers from both system-level and circuit-level perspectives. Following a detailed analysis of the impact of RF imperfections on the performance of the system, we review a number of transceiver and synthesizer architectures that can satisfy the MBOA UWB standard requirements. Next, we describe a new transceiver architecture that accommodates, with three PLLs, the 12 bands specified by the recent MBOA proposal. We also present CMOS circuit techniques for UWB receivers and transmitters and demonstrate a new upconversion path for transmitters that achieves high linearity and low power dissipation. Packaging and testing aspects of the design are also summarized.

I. INTRODUCTION

The principle of ultra-wideband (UWB) communications finds its origin in the 1960s, when it was recognized that some microwave networks could be described more efficiently through impulse response characterization than frequency response measurements [1, 2].¹ Called “impulse,” “carrier-free,” “baseband,” or “time-domain” communications, the method of representing wireless signals by short pulses quickly became popular in military and radar applications, primarily due to low interceptability and fine ranging resolution of such signals. More recently, the prospect of wireless data transmission at rates of hundreds of megabits per second has ignited consumer electronics interest in UWB systems. Examples include the wireless USB and high-definition video streaming. At present, both direct-sequence impulse communications and multiband OFDM UWB systems [3] are under consideration for the standard.

This paper deals with the design of multiband UWB transceivers at the architecture and circuit levels. Section II gives a system overview and Section III analyzes the effect of RF impairments. Sections IV and V respectively derive the design targets and describe transceiver architectures for the first generation. Section VI introduces a new 12-band architecture and Section VII deals with the design of building blocks. Section VIII summarizes packaging and test issues.

¹If excited by an impulse, such networks produce a train of impulses (of varying amplitudes).

II. SYSTEM OVERVIEW

The Multiband OFDM Alliance (MBOA) standard for UWB communications draws heavily upon prior research in wireless local area network (WLAN) systems. In a manner similar to IEEE 802.11a/g, MBOA partitions the spectrum from 3 to 10 GHz into 528-MHz bands and employs OFDM in each band to transmit data rates as high as 480 Mb/s. A significant departure from the original principle of “carrier-free” signaling, the multiband operation is chosen to both simplify the generation and detection of signals and leverage well-established OFDM solutions from WLAN systems. To ensure negligible interference with existing standards, the FCC has limited the output power level of UWB transmitters to -41 dBm/MHz.

Figure 1 shows the structure of the MBOA bands and the channelization within each band. The 14 bands span the range

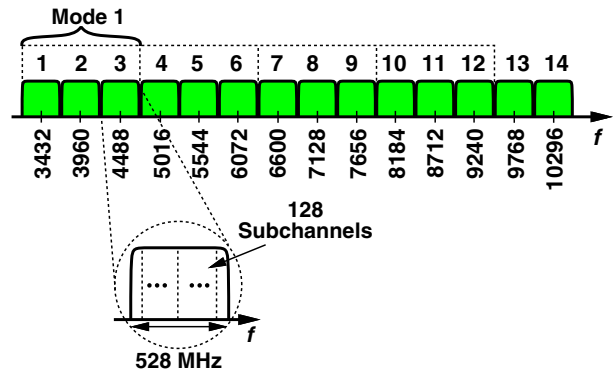


Fig. 1. MBOA band structure and channelization.

of 3168 MHz to 10560 MHz, with their center frequencies given by $m \times (264 \text{ MHz})$ for $m = 13, \dots, 39$. Each band consists of 128 subchannels of 4.125 MHz. In contrast to IEEE 802.11a/g, MBOA employs only QPSK modulation in each subchannel to allow low resolution in the baseband analog-to-digital (A/D) and digital-to-analog (D/A) converters (4-5 bits). Bands 1-3 constitute “Mode 1” and are mandatory for operation whereas the remaining bands are envisioned for high-end products.

In order to improve the robustness of the system with respect to multipath effects and interference, the standard complements OFDM with band hopping. In Mode 1, for example, the information bits are interleaved across all three bands and, as illustrated in Fig. 2, the system hops at the end of each OFDM symbol (every 312.5 ns). The band switching must occur in less than 9.47 ns, thereby posing difficult challenges

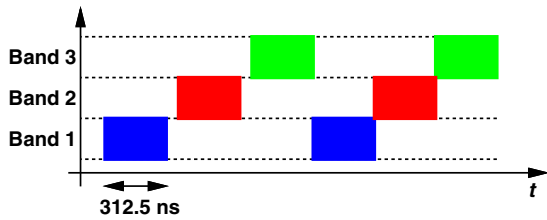


Fig. 2. Band hopping in MBOA.

in the design of the transceiver.

Table 1 compares the receiver (RX) specifications of IEEE 802.11a and MBOA UWB systems for their respective maxi-

	IEEE 802.11a	MBOA UWB
Sensitivity	-65 dBm	-73 dBm
Data Rate	54 Mb/s	480 Mb/s
Channel BW	20 MHz	528 MHz
Modulation	64-QAM	QPSK
SNR (BER = 10^{-5})	23 dB	8 dB
RX NF	12-14 dB	6-7 dB

Table 1. Comparison of IEEE 802.11a and MBOA specifications.

imum data rates.² It is interesting to examine the noise figure (NF) requirements if MBOA had retained the IEEE 802.11a 64-QAM format. To raise the data rate from 54 Mb/s to 480 Mb/s, the channel bandwidth, B , would need to increase from 20 MHz to 178 MHz. Writing

$$\text{Sensitivity} = -174 \text{ dBm} + 10 \log B + \text{NF} + \text{SNR}, \quad (1)$$

and assuming $\text{SNR} = 23 \text{ dB}$ for a bit error rate (BER) of 10^{-5} , we have

$$\text{Sensitivity} = -68.5 \text{ dBm} + \text{NF}. \quad (2)$$

That is, it would have been impossible to achieve a sensitivity of -73 dBm . On the other hand, if SNR is relaxed by reducing the order of the modulation, the sensitivity can be improved even though $10 \log B$ increases to some extent. In particular, with $\text{SNR} = 8 \text{ dB}$ for QPSK modulation and $B = 528 \text{ MHz}$,

$$\text{Sensitivity} = -79 \text{ dBm} + \text{NF}, \quad (3)$$

indicating that an NF of about 6 dB yields the required sensitivity.³

One can attribute the foregoing significant improvement in the sensitivity to Shannon's theorem:

$$C = B \log_2(1 + \text{SNR}), \quad (4)$$

where C denotes the capacity. Since C exhibits a stronger dependence on B than on SNR, it can be concluded that higher data rates are more efficiently afforded by raising the symbol rate (with low-order modulation) than by requiring a high-order modulation (with low symbol rate).

²The MBOA modulation for maximum bit rate has recently changed to "dual-carrier modulation" (DCM) but the required SNR remains the same.

³Owing to the coding gain in the system, the NF can be a few decibels higher.

III. EFFECT OF RF IMPAIRMENTS

As with other RF systems, the performance of UWB transceivers must be quantified in terms of various nonidealities so as to determine the maximum impairment that can be tolerated in each building block. Extensive system-level simulations are therefore carried out with QPSK-modulated OFDM waveforms that are subjected to each nonideality and subsequently detected to provide the resulting bit error rate or packet error rate. The imperfections considered here include I/Q mismatch, oscillator phase noise, and transmitter (TX) output nonlinearity—all for the maximum data rate of 480 Mb/s.

A. I/Q Imbalance

Figure 3 plots the BER as a function of SNR (= symbol energy/noise energy) for various phase and gain mismatches. For reference, the zero-mismatch behavior is also shown. It

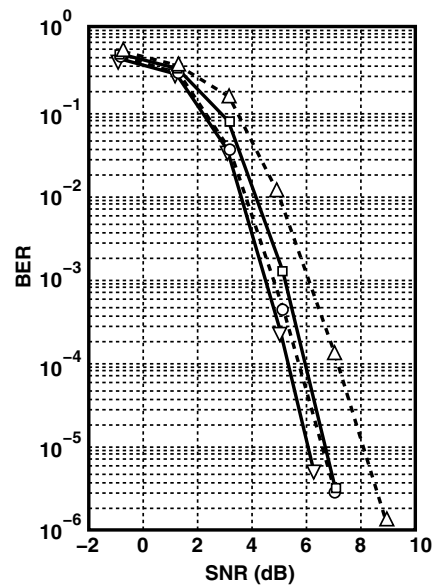


Fig. 3. Effect of I/Q imbalance on BER. (∇ : no imbalance; \circ : $\Delta\phi = 6^\circ$, $\Delta A = 0.6 \text{ dB}$; \square : $\Delta\phi = 10^\circ$, $\Delta A = 0.8 \text{ dB}$; \triangle : $\Delta\phi = 16^\circ$, $\Delta A = 1.4 \text{ dB}$.)

is observed that phase and amplitude mismatches of 6° and 0.6 dB, respectively, degrade the performance by about 0.3 dB. Thus, Mode 1 systems may be able to operate without I/Q calibration, but higher bands are likely to require it.

B. Phase Noise

Figure 4(a) shows the BER as a function of SNR for different oscillator phase noise levels. The phase noise is modeled as shown in Fig. 4(b), with a variable corner frequency, f_c . Since it is anticipated that the frequency synthesizers operate with a reference frequency of $264/4 = 66 \text{ MHz}$ (limited by availability, cost, and phase noise of crystal oscillators), the possibility of $f_c = 5 \text{ MHz}$ is also considered. These results suggest that a plateau phase noise of -100 dBc with $f_c \approx 5 \text{ MHz}$ affects the performance negligibly, making ring oscillators (along with wideband synthesizers) a viable solution.

It is interesting to note that, unlike narrowband RF receivers,

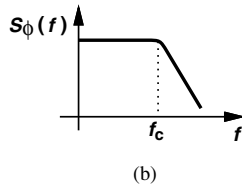
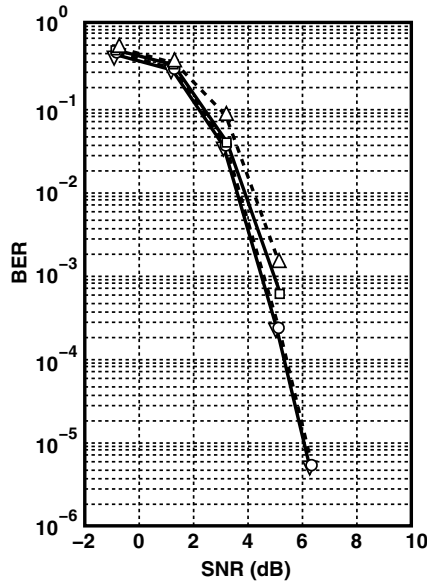


Fig. 4. (a) Effect of phase noise on BER (∇ : $S_{\phi} = 0$; \circ : $S_{\phi} = -100$ dBc/Hz, $f_c = 5$ MHz; \square : $S_{\phi} = -87$ dBc/Hz, $f_c = 924$ kHz; \triangle : $S_{\phi} = -70$ dBc/Hz, $f_c = 924$ kHz), (b) phase noise model.

UWB systems exhibit susceptibility to phase noise primarily in the form of the corruption of the signal constellation; the effect of reciprocal mixing is much less, pronounced because it is determined by the phase noise at an offset of several hundred megahertz. Also, reciprocal mixing due to narrowband interferers (e.g., IEEE 802.11a transmitters) corrupts only a small portion of the channel (Fig. 5).

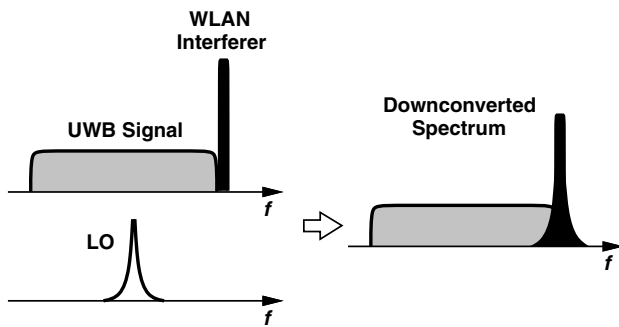


Fig. 5. Effect of reciprocal mixing with a WLAN interferer.

C. TX Nonlinearity

To study the effect of nonlinearity on OFDM signals, a third-order polynomial approximation of the circuit is used. In each simulation, the circuit operates with a certain “backoff” from the output 1-dB compression point. Figure 6 depicts the behavior, suggesting that a backoff of 2-4 dB ensures minimal degradation.

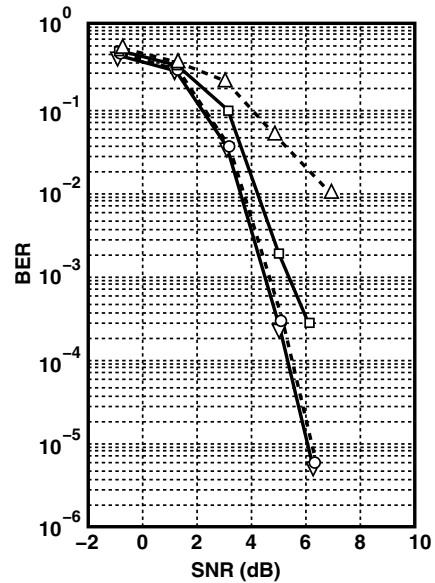


Fig. 6. Effect of nonlinearity on BER. (∇ : 4-dB backoff; \circ : 2-dB backoff; \square : 0-dB backoff; \triangle : -2-dB backoff.)

IV. DESIGN TARGETS

Based on MBOA specifications and the above study of RF impairments, we can now define the required performance of UWB transceivers. We assume direct conversion in both RX and TX paths, but most results apply to other architectures as well.

A. Receiver

Depending on the bit rate, MBOA specifies receiver sensitivities ranging from -84 dBm (for 55 Mb/s) to -73 dBm (for 480 Mb/s). With a required SNR of about 8 dB, these specifications translate to a noise figure of 6-7 dB. The RX must provide a maximum voltage gain of approximately 84 dB so as to raise the minimum signal level to the full scale of the baseband A/D converter. Also, based on the interference expected from IEEE 802.11a/g transmitters, a 1-dB compression point (P_{1dB}) of -23 dBm (in the high-gain mode) is necessary.

Table 2 summarizes the required performance. The phase noise specification is tightened by 5 dB with respect to the value obtained in Section III to allow similar corruption in the transmitter as well. Note that the LNA must accommodate

Sensitivity	-84 to -73 dBm
NF	6-7 dB
P_{1dB}	-23 dBm
I/Q Mismatch	6° and 0.6 dB
Phase Noise	-105 dBc/Hz (Plateau)
Voltage Gain	84 dB
LNA Gain Switch	16-20 dB
Total AGC Range	60 dB
ADC	5-Bit, 528-1056 MHz

Table 2. Required receiver performance.

a gain switch of 16-20 dB to avoid excessive nonlinearity in the OFDM signal (due to the mixer and subsequent stages)

as the received level exceeds -40 dBm. The total range for automatic gain control (AGC) is 60 dB.

The baseband channel-select filter must be designed in conjunction with the A/D converter. Greater stopband rejection provided by the former relaxes the sampling rate of the latter. For example, a third-order Butterworth response necessitates a sampling rate of about $4 \times 264 = 1056$ MHz. The A/D converter resolution is determined by the tolerable quantization noise, the AGC resolution, and the level of WLAN interferers that are only partially attenuated by the filter.

B. Transmitter

The transmitter performance follows corresponding observations in the receiver and is summarized in Table 3.

DAC	5–Bit, 528–1056 MHz
I/Q Mismatch	6° and 0.6 dB
Output Power	-10 dBm
Output P₁ dB	-6 dBm
Carrier Leakage	-30 dBc
Phase Noise	-105 dBc/Hz (Plateau)

Table 3. Required transmitter performance.

V. TRANSCEIVER ARCHITECTURES FOR MODE 1

The design of UWB transceivers faces the following issues: (1) the need for broadband circuits and matching; (2) gain switch in the LNA without degrading the input match; (3) broadband transmit/receive switch at the antenna; (4) desensitization due to WLAN interferers; (5) fast band hopping.

Due to the wide channel bandwidth, the RX and TX paths of UWB systems naturally employ direct conversion rather than, say, low-IF conversion. Typical direct-conversion issues plague the receive path, except that flicker noise negligibly affects the signal. Also, the TX side is free from injection pulling of the oscillator by the output stage because the transmitted level falls below -41 dBm/Hz. (The wide PLL bandwidth also suppresses the pulling [4].)

A. Problem of Band Hopping

As mentioned in Section II, the MBOA standard exploits frequency diversity through band hopping while calling for a settling time of only 9.47 ns. Since typical phase-locked loops (PLLs) take several hundred input cycles to settle, it is not possible to accommodate such fast band switching in a phase-locked synthesizer. This issue dominates the choice of frequency planning.

Another difficulty arising from band hopping relates to offset cancellation in the baseband. On the one hand, the dc offsets change in different bands and, on the other hand, analog offset cancellation circuits that do not attenuate the lowest OFDM subchannels (a few megahertz away from zero) fail to settle in 9.47 ns. For this reason, (coarse) offset cancellation is performed by measuring and digitally storing the offsets for each band during the preamble and applying the results through D/A converters during payload.

B. Frequency Synthesis by Single-Sideband Mixing

In order to generate “agile” local oscillator (LO) signals, two frequencies can be added or subtracted by means of single-sideband (SSB) mixers. Figure 7 depicts an example realized in BiCMOS technology [5]. Here, PLL₁ and PLL₂ produce

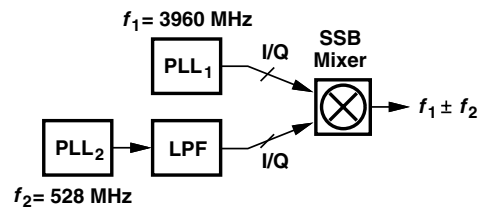


Fig. 7. Generation of Mode 1 frequencies by means of two PLLs. quadrature phases at $f_1 = 3960$ MHz and $f_2 = 528$ MHz, respectively, and subsequent SSB mixers generate $f_1 + f_2$ or $f_1 - f_2$ by a simple polarity change.

SSB mixing, particularly in CMOS technology, presents a number of difficult spur issues. First, at least one port of each “submixer” must be linear to avoid mixing harmonics of that input with those of the other. The required linearization translates to a low conversion gain, small output swings, and hence the need for power-hungry (and perhaps inductor-hungry) buffers. Second, the waveforms applied to the linear ports must themselves exhibit low distortion, a difficult problem at gigahertz frequencies. Third, phase and gain mismatches in the quadrature paths and within the mixers introduce additional spurs. Fourth, dc offsets lead to leakage of the input components to the output.

The BiCMOS design in Fig. 7 must deal with the third harmonic of 528 MHz because the result of mixing this component with 3960 MHz appears at 5544 MHz and 2376 MHz—in or near the WLAN bands. The low-pass filter (LPF) following PLL₂ attenuates this harmonic. (Issues such as conversion gain and phase and gain mismatch are less problematic in bipolar realizations.)

Another interesting embodiment of the above frequency plan is shown in Fig. 8(a) [6]. Here, a single PLL operating at 3960 MHz is followed by a $\div 7.5$ circuit to produce 528 MHz. The challenge lies in the design of a $\div 7.5$ circuit that generates *quadrature* outputs with 50% duty cycle. This is accomplished by two modified versions of the Miller divider. As shown in Fig. 8(b), an SSB mixer and a $\div 2$ constitute a regenerative loop, thereby creating $f_2 = f_1/3$ at the output. Similarly, the topology in Fig. 8(c) serves as a $\div 2.5$ circuit. The operation of each regenerative loop naturally leads to quadrature outputs with 50% duty cycle. Nonetheless, the feedback signals in each case require some filtering so as to approach sinusoids.

In order to avoid SSB mixing, it is possible to employ three PLLs for Mode 1 devices [8]. Illustrated in Fig. 9, the PLLs incorporate ring oscillators to occupy a small area. Since the three frequencies are far from each other and not related by integer multiples, injection pulling is negligible. Note that, even in the presence of coupling between the oscillators (e.g.,

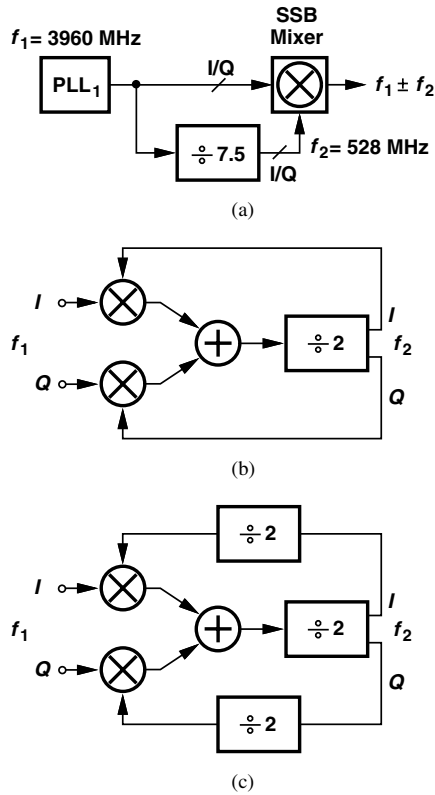


Fig. 8. (a) Generation of Mode 1 frequencies by means of one PLL, (b) realization of $\div 3$ circuit with quadrature outputs, (c) realization of $\div 2.5$ circuit with quadrature outputs.

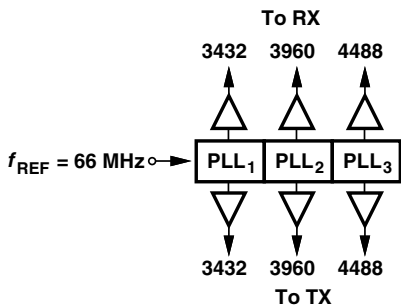


Fig. 9. Generation of Mode 1 frequencies by means of three PLLs.

through the supplies), the spurious components in the WLAN bands remain very small.

Other methods of LO generation are described in [7].

C. Transceiver Example

Figure 10 shows an example of a UWB transceiver designed in 0.13- μm CMOS technology for Mode 1 [8]. (The circuitry in the dashed box contains quadrature components but is drawn with only one phase for clarity.) The receive path consists of an LNA having three resonant loads corresponding to the three bands, with each load driving selectable quadrature mixers. The downconverted signal is applied to a fourth-order Sallen-and-Key (SK) filter and a first-order low-pass stage. An AGC range of 60 dB is distributed as 16 dB in the LNA, 30 dB at the output of the mixers, and 14 dB in the baseband.

The transmit path similarly employs fourth-order SK filters,

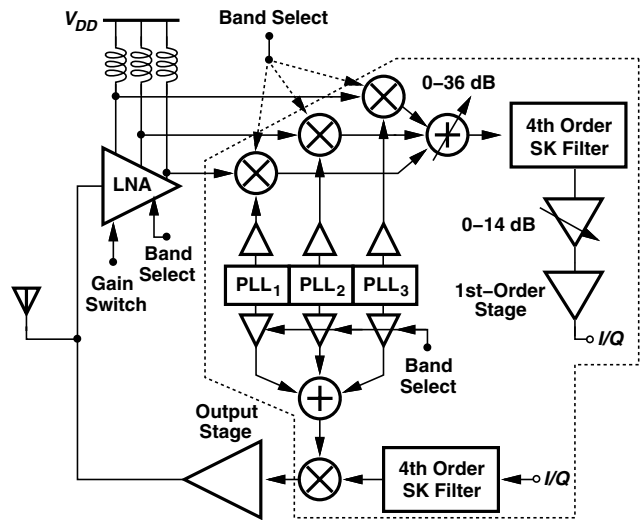


Fig. 10. Mode 1 transceiver architecture.

upconversion mixers, and an output stage that shares the antenna with the LNA. The LO frequencies are synthesized using three independent PLLs to avoid SSB mixing.

It is important to note that the use of a 66-MHz reference frequency for the PLLs allows a loop bandwidth of about 5 MHz, thus suppressing the close-in phase noise of the oscillators considerably. The system therefore can utilize compact ring oscillators.

VI. A 12-BAND TRANSCEIVER ARCHITECTURE

The design issues outlined in Section V for Mode 1 devices prove much more severe as a larger number of MBOA bands are accommodated. In order to cover as many as 14 bands, both a broadband, low-noise signal path and a large set of PLLs and SSB mixers become necessary.

We introduce in this paper a frequency plan that employs only three phase-locked loops to cover the first 12 bands in Fig. 1. Illustrated in Fig. 11(a), the idea is to incorporate two RF PLLs at 5280 MHz and 7392 MHz as the “base” frequencies and add or subtract increments of $(1, 3, 5, 7) \times 264$ MHz to obtain the center frequencies of all of the bands. Figure 11(b) depicts a simplified embodiment of the plan, where each SSB mixer senses one “base” input and one multiplexed increment input. Thus, f_1 covers the center frequencies from 3432 MHz to 7128 MHz, depending on whether the increments are added to or subtracted from 5280 MHz. Similarly, f_2 covers the range 5544 MHz to 9240 MHz. In practice, two sets of this arrangement are necessary so as to produce quadrature LO phases.

Figure 11(c) shows the details of the three-PLL synthesis method. The frequencies $(1, 5, 7) \times 264$ MHz are generated in quadrature form by proper division of the RF PLL outputs.

Of various spurious components produced in the architecture of Fig. 11, three require special attention: (1) $f_{S1} = 7392 \text{ MHz} - 3 \times (1848 \text{ MHz}) = 1848 \text{ MHz}$. This frequency lies within the transmit band of DCS1800 base stations. (2) $f_{S2} = 7392 \text{ MHz} - 3 \times (792 \text{ MHz}) = 5016$

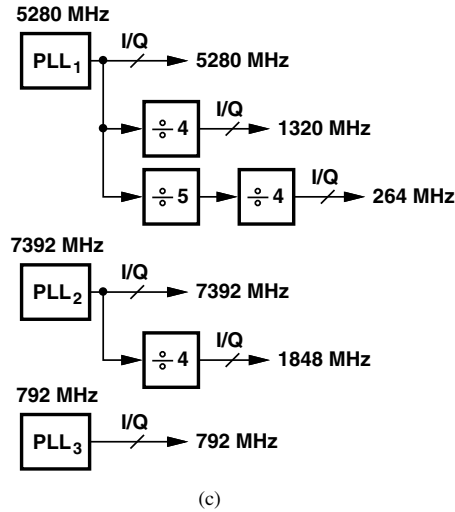
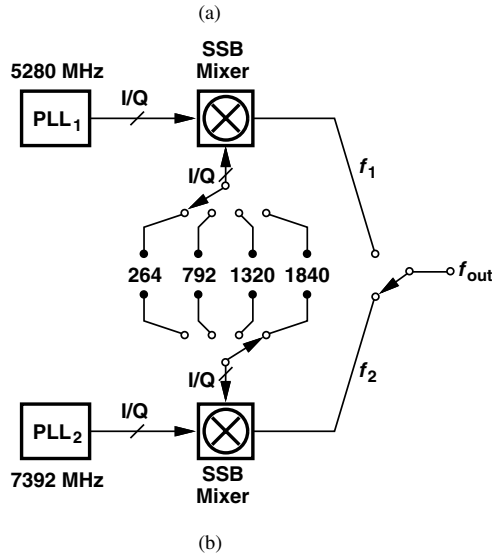
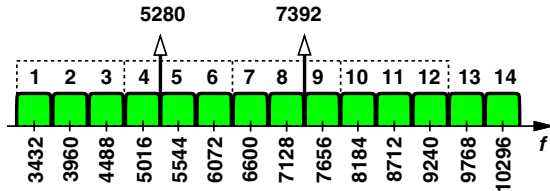


Fig. 11. (a) Choice of "base" frequencies, (b) simplified illustration of frequency synthesis for 12 bands, (c) generation of the base and increment frequencies.

MHz. This frequency is in the vicinity of the first IEEE 802.11a band (5180 MHz-5320 MHz), but still safely far. (3) $f_{S3} = 5280 \text{ MHz} - 3 \times (792 \text{ MHz}) = 2904 \text{ MHz}$. This frequency is 104 MHz above the IEEE 802.11g band. Among these components, only the first appears serious, necessitating filtering of the 1848-MHz signal in Fig. 11(b) to ensure a low third-order harmonic. Note that, by design, the unwanted components arising from phase and gain mismatch fall at the center of the MBOA bands but not on WLAN interferers. For example, the mismatch-induced sideband at $7392 \text{ MHz} - 1848 \text{ MHz} = 5544 \text{ MHz}$ lies outside both IEEE

802.11a bands.

An important issue in the above architecture stems from the multiplexing and routing of quadrature signals at frequencies as high as $f_{2,max} = 9240 \text{ MHz}$. Transistor and interconnect mismatches can introduce substantial phase and gain imbalance here, possibly requiring the use of calibration in the LO and/or RF signal path(s).

VII. CIRCUIT TECHNIQUES

As mentioned in Section V, UWB transceivers present many high-speed design challenges. In addition to oscillators and dividers, the receive and transmit paths also entail difficult design issues.

A. Low-Noise Amplifiers

In addition to typical requirements, the LNA in a UWB system must provide broadband input matching, broadband transfer, and a gain switch of about 16 dB. A UWB LNA example is depicted in Fig. 12 [9], where a Chebychev bandpass

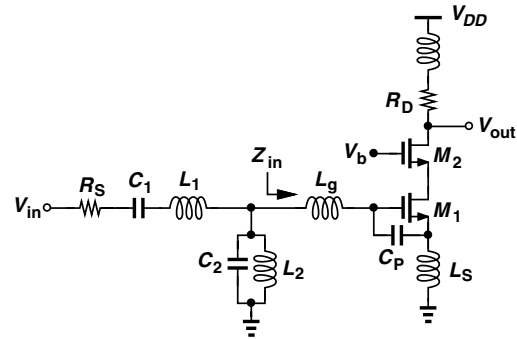


Fig. 12. UWB CMOS LNA.

filter consisting of L_1 , L_2 , C_1 , and C_2 precedes an inductively-degenerated cascode stage, thus cancelling the reactive part of the impedance Z_{in} over a wide band. The circuit achieves a noise figure of 4 dB and a return loss of -10 dB [9].

While providing broadband matching and transfer, the topology of Fig. 12 employs several inductors in the input network and must therefore deal with their loss and noise contribution. Another difficulty is that the required voltage drop across R_D leads to a low gain at lower supply voltages.

An alternative CMOS LNA topology for the Mode 1 bands is shown in Fig. 13 [8]. Here, a common-gate stage provides an input resistance of 50Ω and the large (20-nH) inductor L_1 resonates with the transistor and pad capacitances, yielding adequate return loss across the frequency range. The LNA gain reduction is accomplished by turning M_1 off ($W_1 \approx 8W_2$). The resulting increase in the input resistance is compensated by turning M_6 on. The on-resistance of M_6 varies with process and temperature but the correction still guarantees $|S_{11}| > 10 \text{ dB}$ under all conditions.

Transistors M_3 - M_5 serve as switched cascode devices with tanks resonating at the center frequency of each band. The Q of the tanks is lowered to about 3 to ensure a small droop near the band edges.

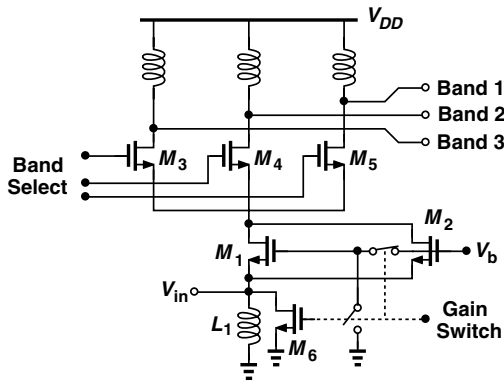


Fig. 13. CG LNA with three resonant loads.

Figure 14 illustrates a bipolar UWB LNA incorporating both current feedback through R_F to broaden the bandwidth of the

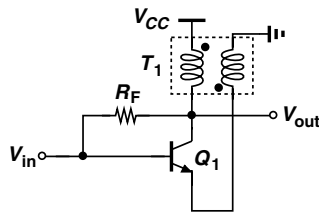


Fig. 14. Bipolar UWB LNA.

input match and voltage feedback through T_1 to improve “noise match” [10].

B. Downconversion Mixers

The mixers in the receive path must provide a variable gain range of about 30 dB. Figure 15 shows an example [8], where the load resistor is decomposed into six binary-weighted seg-

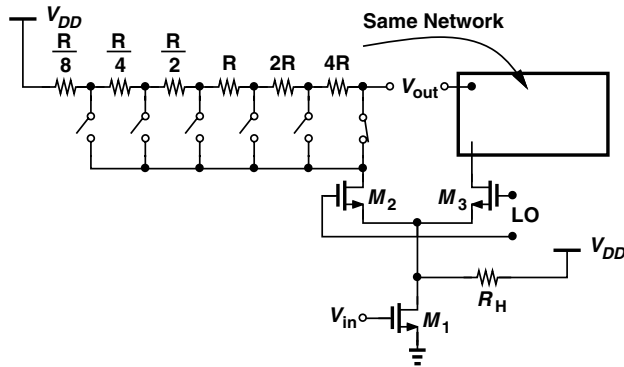


Fig. 15. Downconversion mixer with binary-weighted load.

ments so as to create 6-dB steps in the gain. This gain switching scheme offers (1) a large output bandwidth (> 300 MHz), (2) a high linearity, and (3) a constant output impedance (critical to the design of the subsequent filter).

Resistor R_H in Fig. 15 reduces the bias current commutated by M_2 and M_3 , allowing more abrupt switching and a greater load resistance and hence a higher conversion gain. The common-mode level of the LO port is defined such that R_H carried about half of the bias current of M_1 .

It is possible that the LNA/mixer cascade experiences compression at the *output* of the mixer if the latter provides substantial gain. In this case, the baseband filter can be designed to establish a virtual ground at the mixer output nodes, thereby improving the compression behavior.

C. Baseband Filters

Figure 16(a) depicts an SK filter designed in conjunction with the above mixer. To obtain a flat-band behavior across

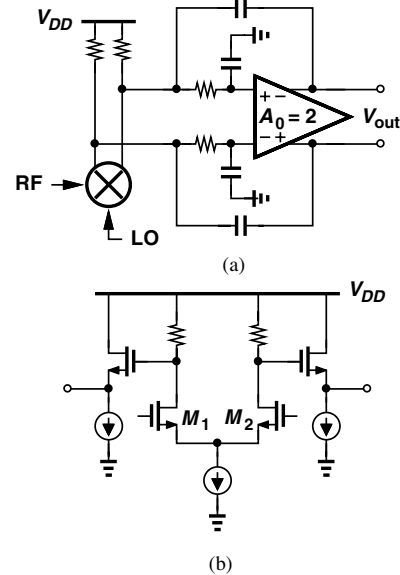


Fig. 16. (a) SK filter topology and its interface with mixer, (b) core amplifier circuit.

300 MHz, the core amplifier is realized as the simple, low-gain circuit of Fig. 16(b). The low loop gain does not force a virtual ground at the mixer output, but the reduction in the voltage swings removes the compression bottleneck from these nodes.

D. Transmitter Circuits

As with WLAN systems, UWB transmitters must deal with RF impairments that degrade OFDM signals, e.g., I/Q mismatches, phase noise, nonlinearity, and carrier feedthrough. Furthermore, a means of output power control is necessary to ensure the transmitted level does not exceed -41 dBm/MHz (-14 dBm across 528 MHz).⁴ Also, it is preferable to avoid an explicit transmit/receive switch for sharing the antenna between the RX and TX paths.

We introduce an upconversion circuit that achieves both a broad bandwidth and high linearity. Depicted in Fig. 17, the circuit employs resistively-degenerated passive mixers along with a current feedback amplifier that creates a virtual ground at the mixer output nodes. The operation can be viewed as voltage-to-current conversion by R_1 and R_2 and current summation at nodes X and Y . An important advantage of using

⁴Recent FCC regulations allow 3 dB higher power in the presence of band hopping.

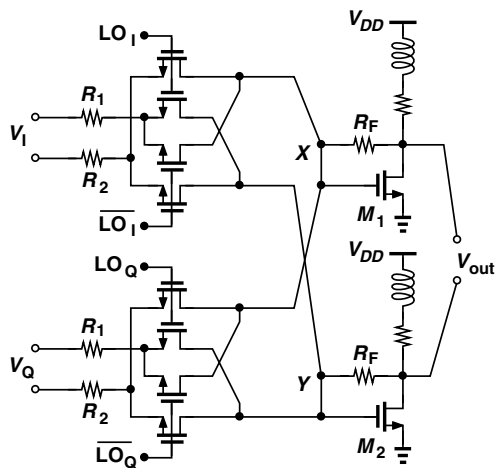


Fig. 17. Linear upconversion path for UWB signals.

passive mixers in the TX path is their zero dc offset as it yields zero carrier feedthrough.⁵

The above circuit achieves an output 1-dB compression point of -3 dBm while drawing 8 mA from a 1.2-V supply.

Figure 18 shows the front end of a UWB CMOS transceiver [8]. Here, a differential to single-ended circuit consisting of

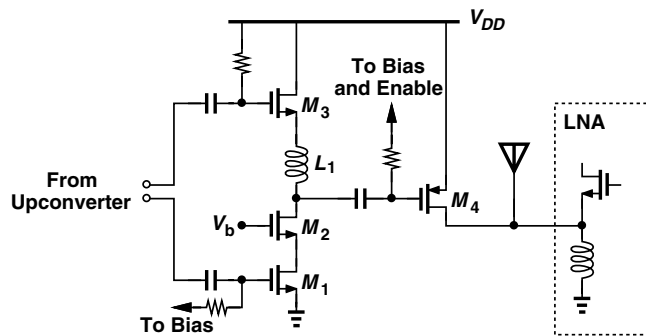


Fig. 18. Front end of a Mode 1 transceiver.

M_1 - M_3 senses the upconverted signal. Inductor L_1 serves as a shunt peaking element for the cascode stage and as a series peaking element for the source follower. Transistor M_4 delivers an output level of -10 dBm to the antenna while the LNA is disabled. Due to the capacitance introduced by M_4 at the antenna port, this RX/TX switching scheme poses a 0.2-dB noise figure penalty on the receiver.

VIII. PACKAGING AND TESTING ISSUES

The broadband interface between the antenna and UWB transceivers makes the package parasitics a critical problem. An effective method of controlling the impedance of this interface is to surround the input bond wire(s) with ground bond wires so as to create a return path and hence a characteristic impedance close to 50Ω . As with other RF systems, accurate modeling of the package and bond wires is essential here.

Another important issue in packaging UWB transceivers relates to the coupling of the oscillators through their shared

⁵Switch mismatches still introduce some carrier feedthrough.

supplies. Since it may not be possible to provide dedicated supply pads and pins to each oscillator, some on-chip filtering is necessary.

The testing of UWB systems requires baseband connections with a bandwidth of greater than 300 MHz. The quadrature OFDM signals applied to the TX or sensed at the output of the RX must travel over traces on test boards with minimal distortion. Also, generation of OFDM signals carrying a data rate of 480 Mb/s may necessitate custom-designed setups such as FPGAs.

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