Nios II Performance Benchmarks

June 2009, version 4.0 Data Sheet

Performance Benchmarks Overview

This data sheet lists the performance and logic element (LE) usage for the Nios® II version 9.0 SP1 soft processor and peripherals. The Nios II soft processor is configurable and designed for implementation in Altera® FPGAs. The following Nios II processors were used for these benchmarks:

- Nios II /f — The Nios II /f "fast" processor is designed for high performance and presents the most configuration options.
- Nios II /s — The Nios II /s "standard" processor is designed for small size while maintaining moderate performance.
- Nios II /e — The Nios II /e "economy" processor is designed to achieve the smallest possible processor size.

The default options for the Nios II processor were chosen for these benchmarks, unless specified otherwise. All of the designs were compiled using the Quartus® II version 9.0 SP1 software.

Your results may vary slightly depending on the version of the Quartus II software, the version of the Nios II processor, and the particular Altera device targeted. Also, any changes to the system logic design may change the performance and LE usage.

Table 1 and Table 2 list the f_{MAX} and millions of instructions per second (MIPS) for a system with the following components:

- Nios II processor (version 9.0 SP1) with JTAG Debug Module
- JTAG UART
- 64 Kbyte on-chip memory (Cyclone® designs use 1 Mbyte of off-chip SDRAM)
- Avalon Memory-Mapped pipeline bridge
- Timer

The MIPS reports were obtained using the MIPS (Dhrystones 2.1 benchmark). You can download the Dhrystones 2.1 benchmark software from *Nios II Embedded Processor Design Examples*. Refer to the **readme.txt** file for further information on the Dhrystones 2.1 benchmark software.

The Fast design example illustrates a system that has all the components listed. You can download the Fast design example from *Nios II Embedded Processor Design Examples*. Refer to the **readme.txt** file for further information on Fast design example.

Table 1. Maximum Clock Frequency (f_{MAX}) for Nios II Processor System (MHz) Note (1)

Device Family	Device Used	Nios II /f	Nios II /s	Nios II /e
Stratix® IV *(2)*	EP4SGX230HF35C2	290	250	340
Stratix III	EP3SL150F1152C2	290	230	340
Stratix II	EP2S60F1020C3	220	170	285
Stratix	EP1S80F1020C5	150	130	170
HardCopy® III *(2)*	HC322FF1152	230	220	210
HardCopy II	HC230F1020C	200	200	320
HardCopy Stratix	EP1S80F1020C5_HC	150	130	175
Cyclone® III	EP3C40F324C6	175	145	215
Cyclone II	EP2C20F484C6	140	110	195
Cyclone	EP1C20F400C6	135	120	175
Arria II® GX *(2)*	EP2AGX95DF25C4	210	190	320
Arria GX	EP1AGX60CF484C6	140	100	150

Notes to Table 1:
(1) These results were generated using seed sweeping and synthesis/fitting settings in the Quartus II software.
(2) Stratix IV, HardCopy III, and Arria II GX results are based on preliminary Timing Models.

Table 2 shows the MIPS value for different types of Nios II processor, while Table 3 shows the ratio of MIPS over system clock (MIPS/MHz).

Table 2. MIPS for Nios II Processor System Note (1) (Part 1 of 2)

Device Family	Device Used	Nios II /f	Nios II /s	Nios II /e
Stratix IV *(1)*	EP4SGX230HF35C2	340	150	48
Stratix III	EP3SL150F1152C2	340	140	48
Stratix II	EP2S60F1020C3	250	110	45
Stratix	EP1S80F1020C5	170	80	27
HardCopy III *(1)*	HC322FF1152	260	140	30
HardCopy II	HC230F1020C	230	130	50
HardCopy Stratix	EP1S80F1020C5_HC	165	85	27
Cyclone III	EP3C40F324C6	195	90	30
Cyclone II	EP2C20F484C6	145	55	18

Table 2. MIPS for Nios II Processor System Note (1) (Part 2 of 2)

Device Family	Device Used	Nios II /f	Nios II /s	Nios II /e
Cyclone	EP1C20F400C6	130	52	17
Arria II GX *(1)*	EP2AGX95DF25C4	240	120	50
Arria GX	EP1AGX60CF484C6	150	65	25

Notes to Table 2:
(1) These results were generated using seed sweeping and synthesis/fitting settings in the Quartus II software.
(2) Stratix IV, HardCopy III, and Arria II GX MIPS results are based on estimations.

Table 3 shows the ratio of MIPS over system clock (MIPS/MHz).

Table 3. MIPS/MHz Ratio for Nios II Processor System on Various Device Families

Device Family	Nios II /f	Nios II /s	Nios II /e
Stratix IV	1.183	0.611	0.138
Stratix III	1.183	0.611	0.138
Stratix II	1.183	0.611	0.138
Cyclone III	1.109	0.604	0.138
Cyclone II	1.105	0.518	0.107

Table 4 lists the LE usage for the Nios II processor cores and most of the common peripherals for Stratix IV, Stratix III, Stratix II, and Stratix devices.

Table 4. Logic Element Usage for Nios II Processor Cores and Peripherals — Stratix IV, Stratix III, Stratix II, and Stratix Devices Note (1) (Part 1 of 2)

Processor Core / Peripheral	Stratix IV (ALUTs) *(1)*	Stratix III (ALUTs)	Stratix II (ALUTs)	Stratix (LEs)
Nios II /f *(3)*	1,020	1,020	1,320	1,800
Nios II /s *(4)*	850	800	1,030	1,170
Nios II /e *(5)*	520	520	500	530
Nios II JTAG Debug Module	110	110	430	390
UART	40	40	130	150
JTAG UART	115	115	205	210
SDR SDRAM Controller	310	310	520	760

Table 4. Logic Element Usage for Nios II Processor Cores and Peripherals — Stratix IV, Stratix III, Stratix II, and Stratix Devices Note (1) (Part 2 of 2)

Processor Core / Peripheral	Stratix IV (ALUTs) (1)	Stratix III (ALUTs)	Stratix II (ALUTs)	Stratix (LEs)
Timer	120	120	185	160

Notes to Table 4:
(1) Resource utilization results for Stratix IV and Stratix III devices were generated using moderate synthesis/fitting settings in the Quartus II software. No seed sweeping was performed, so these results represent typical results. Your results may vary.
(2) An adaptive look-up table (ALUT) is the cell used in the Quartus II software for logic synthesis for Stratix II and later device families. It is equivalent to about 1.25 LEs.
(3) The Nios II/f processor used has 512 bytes instruction and data caches, and no hardware multiplier.
(4) The Nios II/s processor used has 512 bytes instruction, no data caches and hardware multiplier.
(5) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.

Table 5 lists the LE usage for the Nios II processor cores and most of the common peripherals for HardCopy II, HardCopy Stratix, Cyclone III, Cyclone II, and Cyclone devices.

Table 5. Logic Element Usage for Nios II Processor Cores and Peripherals — HardCopy II, HardCopy Stratix, Cyclone III, Cyclone II, and Cyclone Devices Note (1)

Processor Core / Peripheral	HardCopy II (HCells) (2)	HardCopy Stratix (LEs)	Cyclone III (LEs)	Cyclone II (LEs)	Cyclone (LEs)
Nios II /f (3)	8,900	1,770	1,800	1,600	1,680
Nios II /s (4)	6,500	1,200	1,300	1,030	1,140
Nios II /e (5)	2,250	520	650	540	520
Nios II JTAG Debug Module	350	390	250	450	450
UART	520	150	75	140	155
JTAG UART	620	210	170	165	200
SDR SDRAM Controller	1,740	760	420	750	760
Timer	700	160	150	150	155

Notes to Table 5:
(1) Resource utilization results for HardCopy II and Cyclone III devices were generated using moderate synthesis/fitting settings in the Quartus II software. No seed sweeping was performed, so these results represent typical results. Your results may vary.
(2) HCells are logic blocks that implement both logic and DSP functions. DSP block functions are implemented using HCells instead of dedicated DSP blocks.
(3) The Nios II/f processor used has 512 bytes instruction and data caches, and no hardware multiplier.
(4) The Nios II/s processor used has 512 bytes instruction, no data caches and hardware multiplier.
(5) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.

Table 6 lists the LE usage for the Nios II processor cores and most of the common peripherals for HardCopy III, Arria II GX, and Arria GX devices.

Table 6. Logic Element Usage for Nios II Processor Cores and Peripherals — HardCopy III, Arria II GX, and Arria GX Devices *Note (1)*

Processor Core / Peripheral	HardCopy III (HCells) *(2)*	Arria II GX (ALUTs) *(3)*	Arria GX (ALUTs)
Nios II /f *(4)*	9,100	980	1,000
Nios II /s *(5)*	6,900	790	800
Nios II /e *(6)*	4,000	590	550
Nios II JTAG Debug Module	1,200	110	110
UART	700	100	100
JTAG UART	850	110	110
SDR SDRAM Controller	1,900	300	300
Timer	800	110	110

Notes to Table 6:

(1) Resource utilization results for HardCopy III, Arria II GX, and Arria GX devices were generated using moderate synthesis/fitting settings in the Quartus II software. No seed sweeping was performed, so these results represent typical results. Your results may vary.

(2) HCells are logic blocks that implement both logic and DSP functions. DSP block functions are implemented using HCells instead of dedicated DSP blocks

(3) An adaptive look-up table (ALUT) is the cell used in the Quartus II software for logic synthesis for Stratix II and later device families. It is equivalent to about 1.25 LEs.

(4) The Nios II/f processor used has 512 bytes instruction and data caches, and no hardware multiplier.

(5) The Nios II/s processor used has 512 bytes instruction, no data caches and hardware multiplier.

(6) The Nios II/e processor used has no instruction, data caches, and hardware multiplier.

Additional performance benchmarking information for Nios II processor can be found at these links:

- On Nios II interrupt latency performance, refer to the *Exception Handling* chapter in the *Nios II Software Developer's Handbook*.
- On Nios II floating-point custom instruction performance, see *Using Nios II Floating-Point Custom Instructions Tutorial*.
- On Nios II networking applications performance, see *AN440: Accelerating Nios II Networking Applications*.

Document Revision History

Table 7 shows the revision history for this document.

Table 7. Document Revision History

Date and Document Version	Changes Made	Summary of Changes
June 2009 v4.0	• Measured performance and LE usage with the Quartus II version 9.0 SP1 software and the Nios II version 9.0 SP1 processor • Added information for the HardCopy III, Arria II GX, and Arria GX devices	Updated Tables 1 and 2 with new data. Added Table 6.
July 2008 v3.0	• Measured performance and LE usage with the Quartus II version 8.0 software and the Nios II version 8.0 processor • Added information for the Stratix IV device • Added links for additional information on Nios II benchmark performance	Updated Tables 1, 2, 4 and 5 with new data. Added Table 3.
August 2007 v2.0	• Measured performance and LE usage with the Quartus II version 6.1 software and the Nios II version 6.1 processor • Added information for the Stratix III, HardCopy II, and Cyclone III devices	Updated Tables 1, 2, and 3 with new data.
October 2004 v1.0	Initial release	—

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