Features

- **High Performance ULC Family Suitable for Latest CPLDs and FPGAs conversion**
- **Very effective associated Physical synthesis/optimization Flow**
- **From 45K Gates up to 1000K Gates Supported**
- **From 55Kbit to 847Kbit DPRAM**
- **Compatible with Xilinx and Altera Latest FPGA's**
- **Pin-count: Over 700 pins**
- **VDD 1.8V +/- 0.15V for core; 1.8V, 2.5V, 3.3V for Periphery**
- **Any Pin–out Matched**
- **Full Range of Packages: PQFP/TQFP/VQFP, BGA/FLBGA, PGA/PPGA, QFN, CS**
- **Available in Commercial, Industrial and Military Grades**
- **0.18 um Drawn CMOS, 5 Metal Layers**
- **Library Optimised for best Synthesis, Place & route and Testability Generation (ATPG)**
- **High system clock Skew Control**
- **250Mhz system clock, up to 400Mhz for local clock**
- **Power on Reset, PLL, Multiplier**
- **Standard 3, 6, 12, 24 mA I/Os**
- **LVCMOS, LVTTL, GTL, HSTL, LVPECL, PCI & LVDS Interfaces**
- **High Noise & EMC Immunity**
- **Thick Oxide periphery Allowing Interface with 2.5V and 3.3V Environments**

Description

The ATU18 series of ULCs are fully suited for conversion of latest CPLDs and FPGAs. It supports within one ULC 55Kbits to 847Kbits DPRAM and 45Kgates to 1000 Kgates. Typically, ULC die size is 50% smaller than the equivalent FPGA. Metal level customisation allows a DPRAM blocks compatibility with Xilinx® or Altera® blocks.

Devices are implemented in high–performance 0.18 um CMOS technology to improve the design frequency and reach 250Mhz typical application and local clock up to 400Mhz. The architecture of the ATU18 series is dedicated for efficient conversion of latest CPLD and FPGA device types with higher IO count. A compact RAM cell and a large number of available gates allow the implementation of memories compatible with FPGA RAM, as well as JTAG boundary–scan and scan–path testing.

Conversion to the ATU18 series of ULC provides a significant reduction of the operating power when compared to the original PLD or FPGA. The ATU18 series has a very low standby consumption, less than 0.145 nA/gate typically at commercial temperature. Operating consumption is a strict function of clock frequency, which typically results in a significant power reduction depending on the device being compared. For a NAND2 cell the dynamic power consumption is 0.124uW/MHz at 1.8V.

0.18 um ULC Series with Embedded DPRAM

ATU18

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The ATU18 series provide several options for output buffers, including a variety of drive levels up to 24mA. Schmitt trigger inputs are also available. A number of techniques are used to improve noise immunity and to reduce EMC emissions, including several independent power supply buses and internal decoupling for isolation.

The ATU18 series are designed to allow conversion of high performance 1.8V devices. Support of mixed supply conversions is also possible, allowing optimal trade–offs between speed and power consumption.

Array Organization

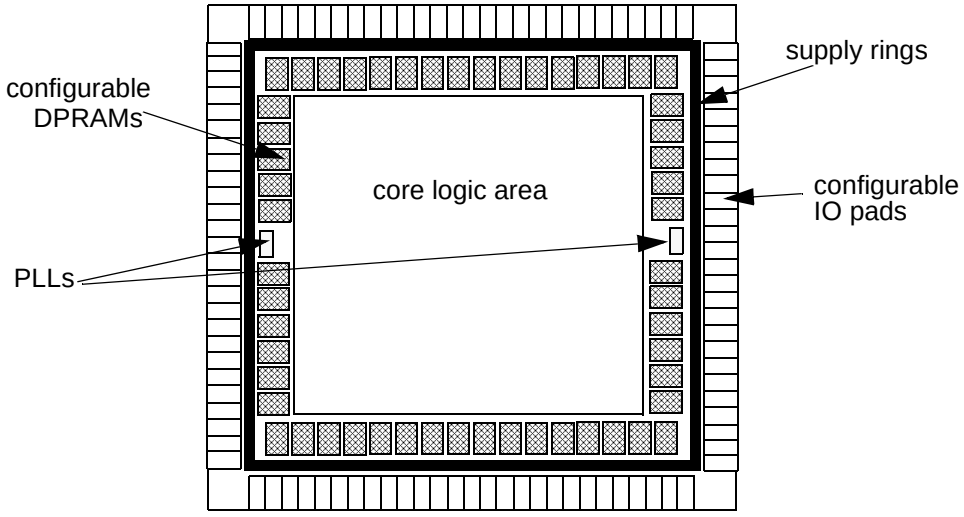
Table 1. Matrices

Part Number	Max Pads	Gates	DPRAM bits	PLL
ATU18_680	680	1000K	847K	4
ATU18_600	600	720K	700K	4
ATU18_484	484	486K	460K	2
ATU18_432	432	330K	350K	2
ATU18_352	352	276K	221K	2
ATU18_304	304	171K	183K	2
ATU18_256	256	111K	147K	2
ATU18_160	160	45K	55K	1

Architecture

The ATMEL 0.18um matrices allow conversions of designs being developed on Altera/Apex-Apex™II Stratix® Cyclone™ or Xilinx/Virtex™, Spartan™ and CoolRunner™ families. Each matrix contains configurable memory DPRAM blocks, PLLs (from 2 to 4) and Power-on-Reset. It can also integrate a 1.8V regulator from 3.3V supply if no available 1.8V on the board. The associated Physical synthesis/optimization flow contributes to achieve high speed designs, even improving drastically the application frequency and power consumption.

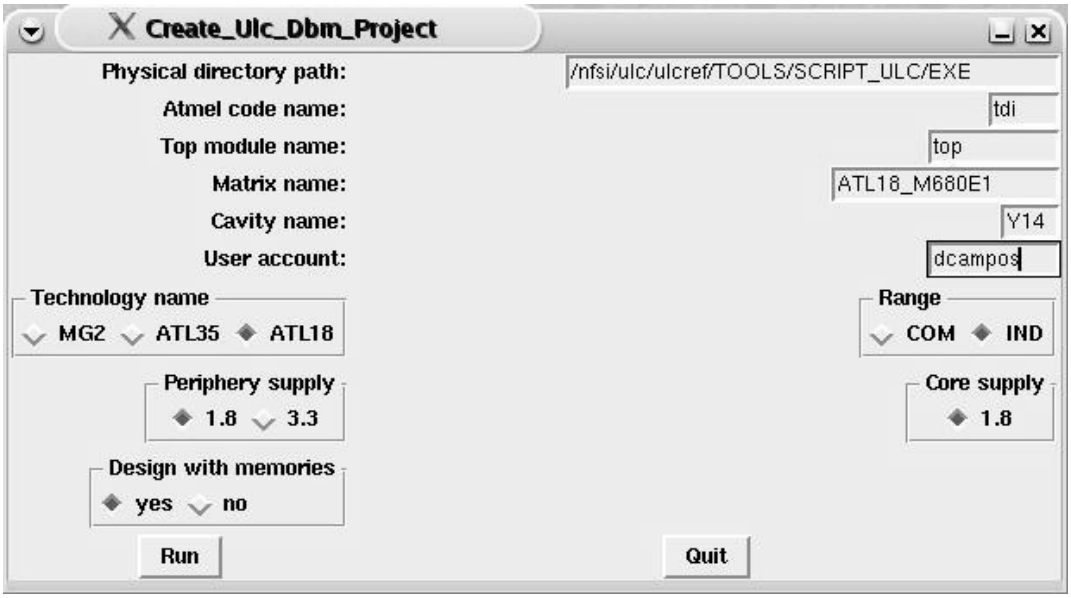
Figure 1. Atmel 0.18um matrix



DPRAM Description

For flexibility, the embedded DPRAMs blocks, using an ATMEL memory configuration tool, are configured at customization Metal levels, in order to match behaviour and format of Xilinx or Altera memories.

Figure 1. ATMEL Memory Configuration Tool



For test in production, a bist is systematically inserted, without degrading the performances. The memories will be then automatically tested to provide high reliability.

Table 2. Dual Port Mode Configurations

Memory area 576k bits					Memory Area 18K bits					
Port A	**64kx9**	**64kx9**	**64kx9**	**64kx9**	**16kx1**	**16kx1**	**16kx1**	**16kx1**	**16kx1**	**16kx1**
Port B	**64kx9**	**32kx18**	**16kx36**	**8Kx72**	**16kx1**	**8kx2**	**4kx4**	**2kx9**	**1kx8**	**512x36**
Port A	**32kx18**	**32kx18**	**32kx18**		**8kx2**	**8kx2**	**8kx2**	**8kx2**	**8kx2**	
Port B	**32kx18**	**16kx36**	**8kx72**		**8kx2**	**4kx4**	**2kx9**	**1kx18**	**512x36**	
Port A	**16kx36**	**16kx36**			**4kx4**	**4kx4**	**4kx4**	**4kx4**		
Port B	**16kx36**	**8kx72**			**4kx4**	**2kx9**	**1kx18**	**512x36**		
Port A	**8kx72**				**2kx9**	**2kx9**	**2kx9**			
Port B	**8kx72**				**2kx9**	**1kx18**	**512x36**			
Port A	**4Kx144**				**1kx18**	**1kx18**				
Port B	**4Kx144**				**1kx18**	**512x36**				
Port A					**512x36**					
Port B					**512x36**					

I/O Buffer Interfacing

I/O Flexibility

All I/O buffers at the periphery may be configured as input, output, bi-directional and oscillator. The IO power rings can be modified to allow clusterization (i.e. cluster at 1.8V cluster at 3.3V).

When core supply differs from periphery supply, level shifters are available in IO buffers, for example in the following conditions:

3.3V I/O -> 1.8V core,
2.5V I/O->1.8V core.

Each LVTTL, LVCMOS, or Schmitt Trigger input can be programmed with or without a pull up or pull down resistor or bus keeper. The Standard IO supported are given in table 3.

Fast Output Buffer are able to drive 3 to 24mA at 3.3V according to the chosen option. (higher drive is achievable using two adjacent pads).

Table 3. Standard IO Supported

Standard IO	Comment
LVTTL	3.3V (3 to 24 mA)
LVCMOS	1.8V/2.5V/3.3V (3 to 24 mA)
PCI33	3.3V
PCI66	3.3V
GTL	3.3V
GTL+	3.3V
HSTL I, II, III, IV	input only
SSTL2 I, II	input only
SSTL3	input only
LVPECL	input only
LVDS	3.3V

PLL Description

ATMEL PLL is available for a large range of frequencies. It has an internal filter and no external component is necessary.

Programming at customization level allows to choose between four ranges of VCO frequency as shown in the table below:

FreqSelect1	FreqSlect0	VCO Frequency
0	0	66-90Mhz
0	1	90-160Mhz
1	0	155-300Mhz
1	1	280-500Mhz

Different outputs are also available, to ensure a wide variety of use. The drawing below shows the IOs of the PLL.

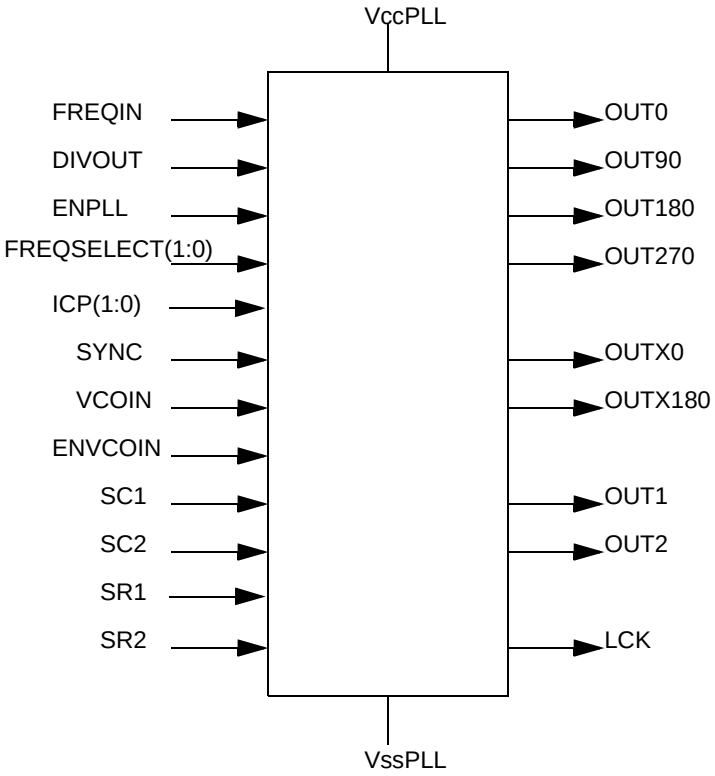


Table 4. Pin Description

Pin Name	TYPE	I/O	Function
FREQIN	digital	I	Reference input frequency
DIVOUT	digital	I	Feedback input frequency
FREQSELECT(1:0)	digital	I	VCO frequency range select
SC2,SC1	digital	I	internal filter value select
ICP(1:0)	digital	I	Charge pump current select

Table 4. Pin Description

Pin Name	TYPE	I/O	Function
SR1, SR2	digital	I	internal filter value select
SYNC	digital	I	synchronization mode select
VCOIN	analog	I	VCO external input
ENVCOIN	digital	I	VCO external input select
OUT0	digital	O	0 degree phase shift of VCO freq divided by 4
OUT90	digital	O	90 degree phase shift of VCO freq divided by 4
OUT180	digital	O	180 degree phase shift of VCO freq divided by 4
OUT270	digital	O	270 degree phase shift of VCO freq divided by 4
OUTX0	digital	O	0 degree phase shift of VCO freq divided by 2
OUTX180	digital	O	180 degree phase shift of VCO freq divided by 2
OUT1	digital	O	VCO output
OUT2	digital	O	delayed VCO output from OUT1
LCK	digital	O	lock output
VCCPLL	power	I	VDD 1.8V pin
VSSPLL	power	I	VSS pin

VCO FREQUENCY	OUT1,OUT2	OUTX0, OUTX180	OUT[0,90,180,270]
66-90Mhz	66-90Mhz	33-45Mhz	16.5-22.5Mhz
90-160Mhz	90-160Mhz	45-80Mhz	22.5-40Mhz
155-300Mhz	155-300Mhz	77.5-150Mhz	38-75Mhz
280-500Mhz	280-500Mhz	140-250Mhz	70-125Mhz

PLL Applications

ATMEL PLL is configurable to support applications as:

- Clock tree delay reduction
- Zero delay buffer
- Phase shift
- Frequency synthesis

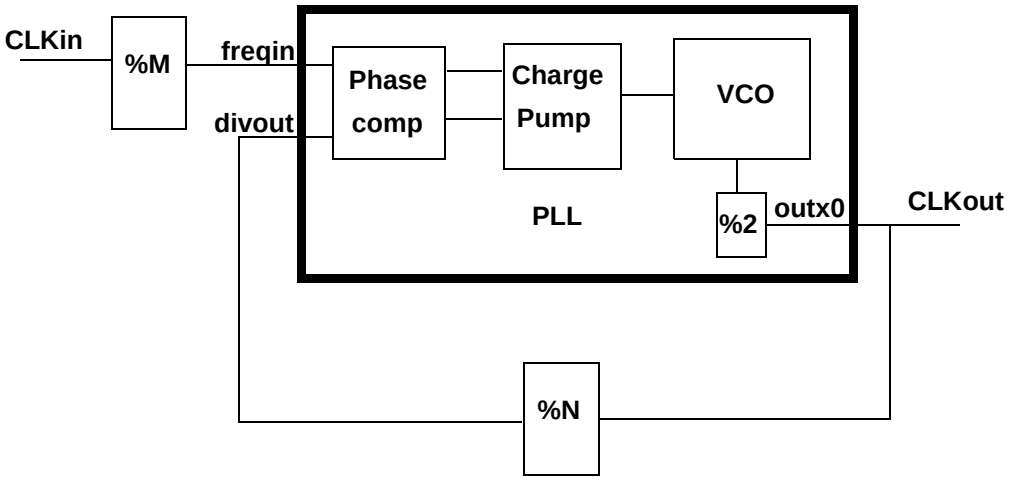
Clock Tree Delay Reduction

Typically, clock tree synthesis is able to build a very performant clock tree (for example: 0.15ns of skew for a clock tree connected to 25000 Flipflops). For that, however, the clock tree latency is increased during clock tree insertion. To satisfy Tco propagation delay, the PLL can be used to reduce and even remove the clock tree delay.

Frequency Synthesis

By adding dividers on input clock and feedback clock, the PLL can be used to multiply the input frequency by a factor determined by the user, as illustrated below:

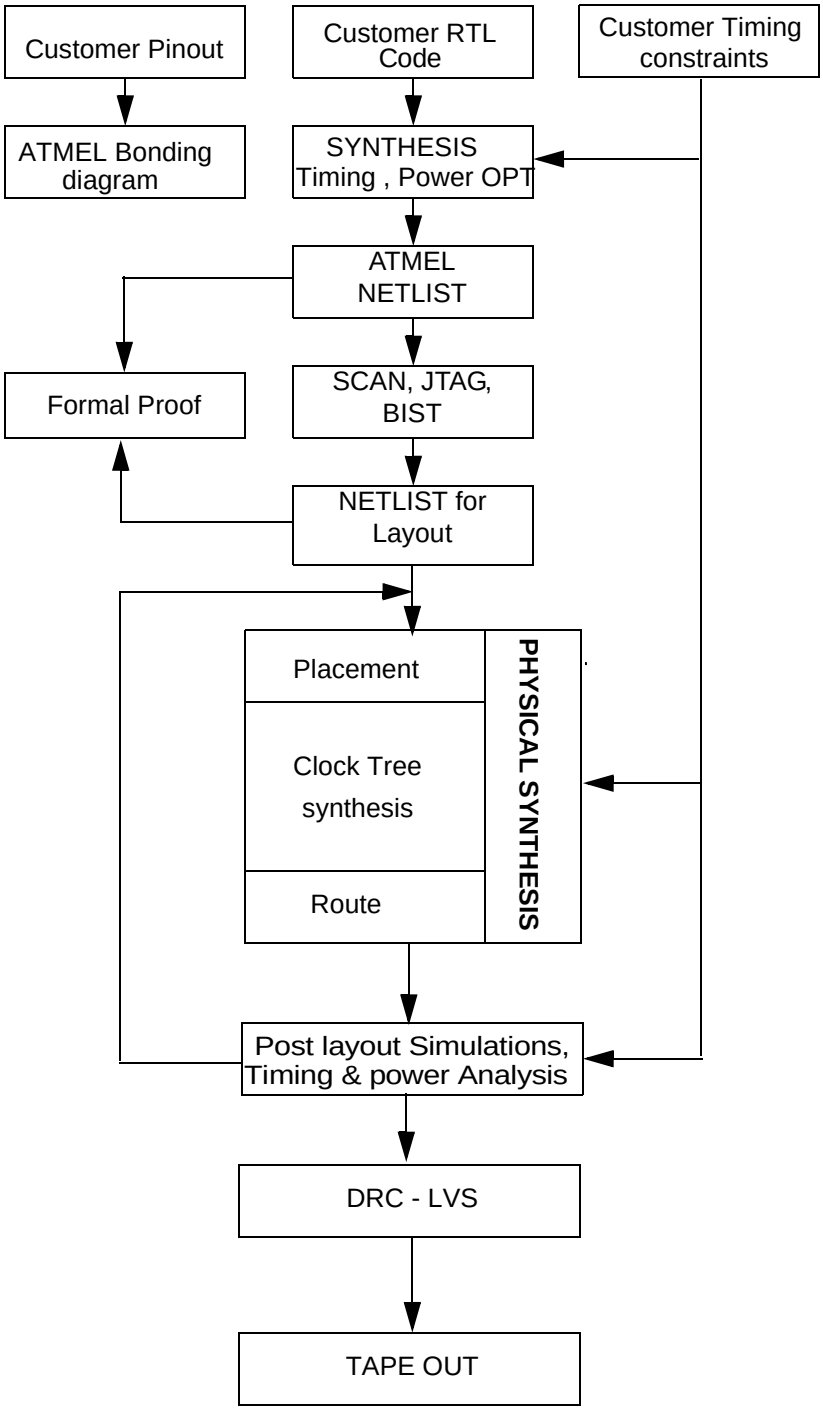
Figure 3. PLL Frequency Synthesis



For example, with a 32Mhz input clock, to generate a 160 Mhz frequency clock on the output outx0, it is necessary to set the input clock divider M to 1 and the feed-back clock divider N to 10.

Atmel Flow

With **0.18um technology**, ATMEL has introduced **Physical synthesis** to optimize design speed. Physical synthesis takes into account the placement and the routing of the cells, and the optimization in incremental mode can be done on the full design or only partially. The result is that ATMEL has faster chips, using the same RTL code. Less iterations are necessary and the timings target is quickly reached.



ATU18 Packages

The following packages are supported:

	ATU18_680	ATU18_600	ATU18_484	ATU18_432	ATU18_352	ATU18_304	ATU18_256	ATU18_160
100 TQFP								
144 TQFP								
100 PQFP								
160 PQFP								
208 PQFP								
240 PQFP								
304 PQFP								
100 FLBGA								
144 FLBGA								
256 FLBGA								
324 FLBGA								
456 FLBGA								
484 FLBGA								
556 FLBGA								
672 FLBGA								
676 FLBGA								
680 FLBGA								
780 FLBGA								
860 FLBGA								
900 FLBGA								
1020 FLBGA								
1156 FLBGA								
1508 FLBGA								
225 BGA								
256 BGA								
313 BGA								
329 BGA								
352 BGA								
356 BGA								
432 BGA								
560 SBGA								
600 SBGA								
652 SBGA								

gray cells : supported package configuration

Remark: Other package and package/matrix configurations can be supported upon request

Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature	
Commercial	0° to 70°C
Industrial	-40° to 85°C
Military	-55° to 125°C
Max Supply Core Voltage (V_{DD})	1.95 V
Max Supply Periphery Voltage (V_{CC})	3.6V
3.3V Tolerant/Compliant	Vcc +0.3V
Pad pullup resistor	100Kohms
Pad pulldown resistor	100Kohms
Output buffer drive range	3 to 24 mA
leakage current at Temp=25C	0.145nA/gate
NAND2 dynamic power consumption	0.124uW/MHz at 1.8V
Storage Temperature	-65° to 150°C

*NOTICE: Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

This value is based on the maximum allowable die temperature and the thermal resistance of the package.

PLL Specifications

Operating Modes

- Clock tree reduction
- Zero delay buffer
- Phase shift
- Frequency synthesis

VCO range	66Mhz to 500Mhz
OUT1, OUT2 output range	66Mhz to 500 Mhz
OUTX0, OUTX180 ouput range	33Mhz to 250 Mhz
OUT0,90,180,270 output range	16.5Mhz to 125Mhz
VDDPLL supply	1.8V +- 10%

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