digitally mastering the spectrum

Scalable & Reconfigurable Software Defined Radio: Digital Front-End Architecture FOR Wideband Channelizer

TU Delft

Computer Engineering

EONIC

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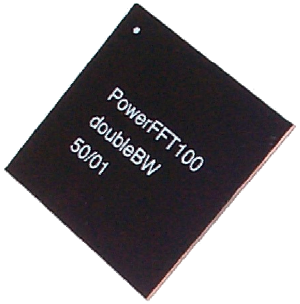
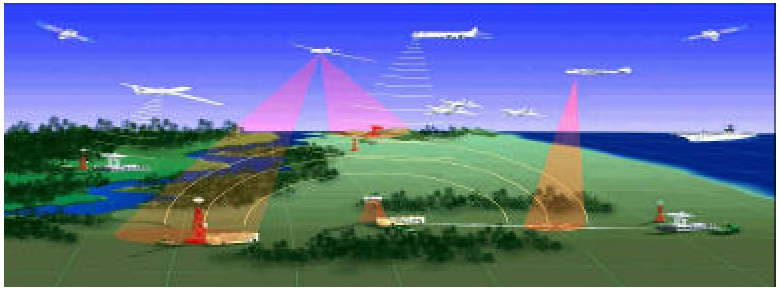
What EONIC BV does?

- PowerFFT – World’s fastest FFT-coprocessor



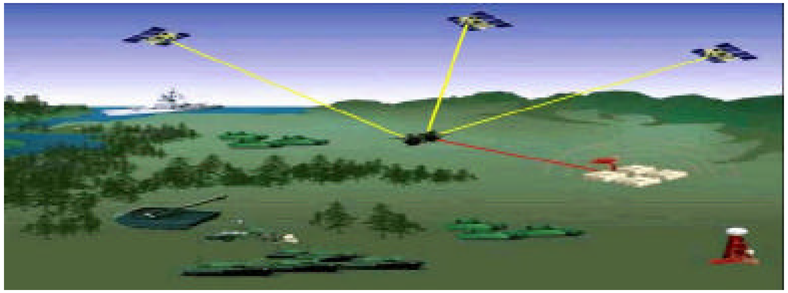
SAR

ESM



DAR

SDR



Problem Statement & Methodology

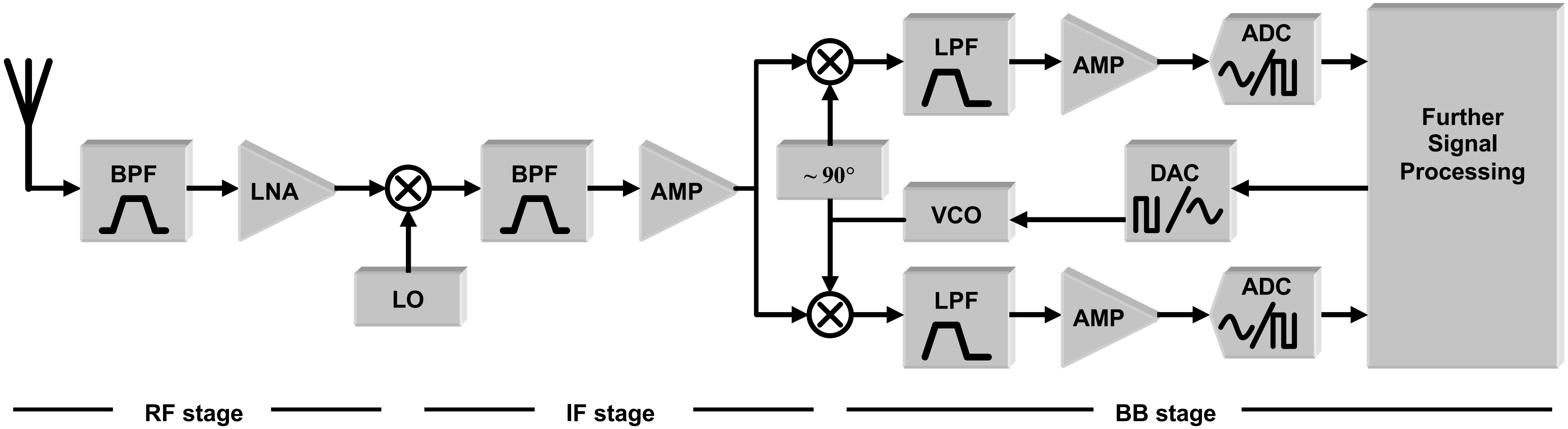
- How to improve critical functionalities in WB SDR digital front-end?
- Phase 1 – Investigating existing channelization algorithms
  - Literature study
  - Comparison & algorithm choice for implementation
- Phase 2 – Investigating critical functionalities
  - Parameterized Matlab® model
  - Test case & critical functionalities choice
- Phase 3 – Implementation
  - Implementing critical functionalities
  - Optimization & evaluation

Presentation Outline

- Introduction
  - What is SDR?
  - SDR Channelization & Applications
- Channelization Algorithms
  - 3 Algorithms
  - Comparison & Conclusions
- Polyphase FFT Wideband Channelizer Architecture
  - Matlab® demonstration

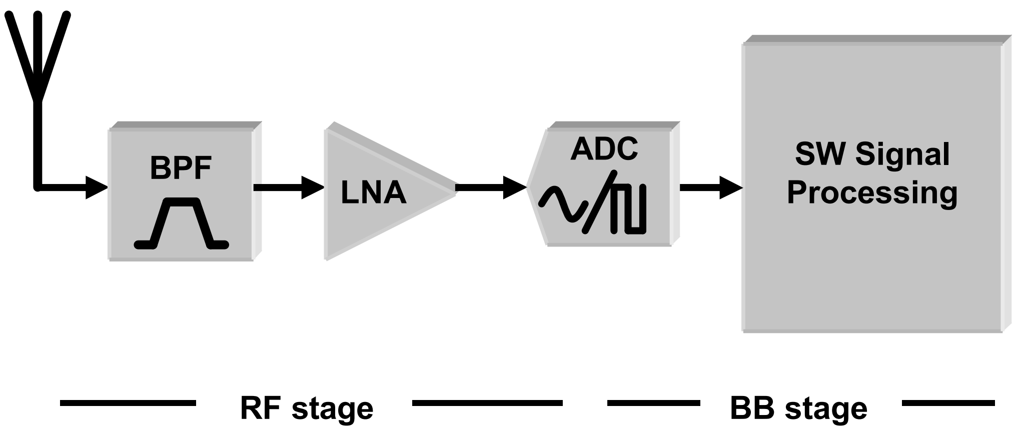
Introduction: What is SDR?

- Traditional Radio Receiver



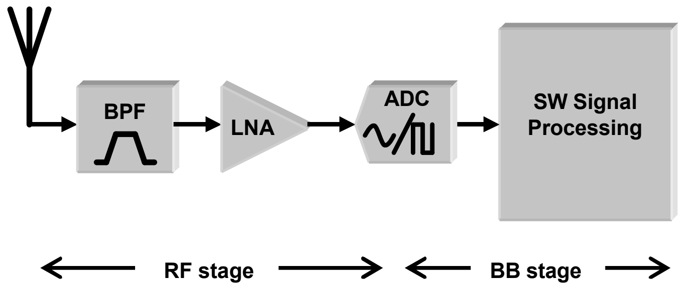
Ideal SDR

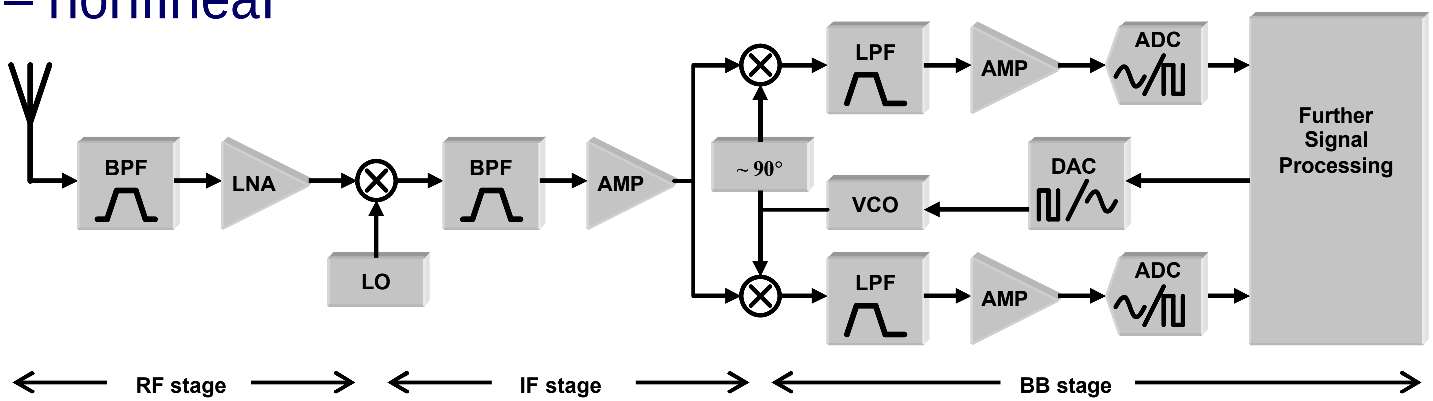
- Digitization as close as possible to the antenna
- Further processing by software



Ideal SDR Receiver vs. Traditional Receiver

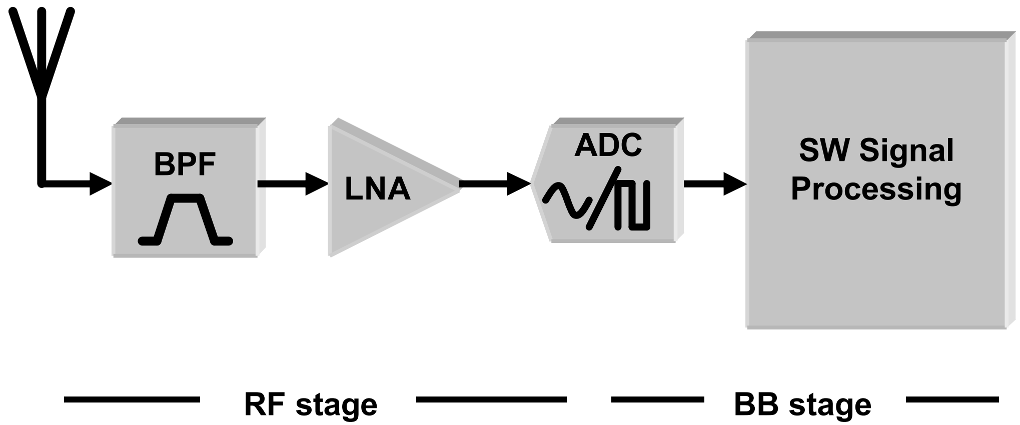
- Why do we need SDR?
- Flexibility - reprogrammable
- Analog components:
  - inaccurate
  - nonlinear





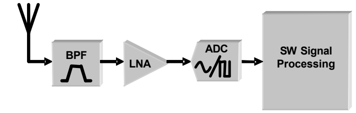
Ideal SDR Receiver Limitations

- Antenna
- ADC
  - Sampling Rate, Resolution, Jitter, Noise
- Computing Capacity

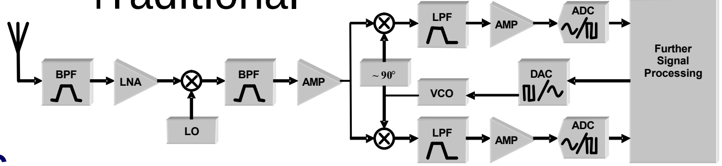


Intermediate Solution

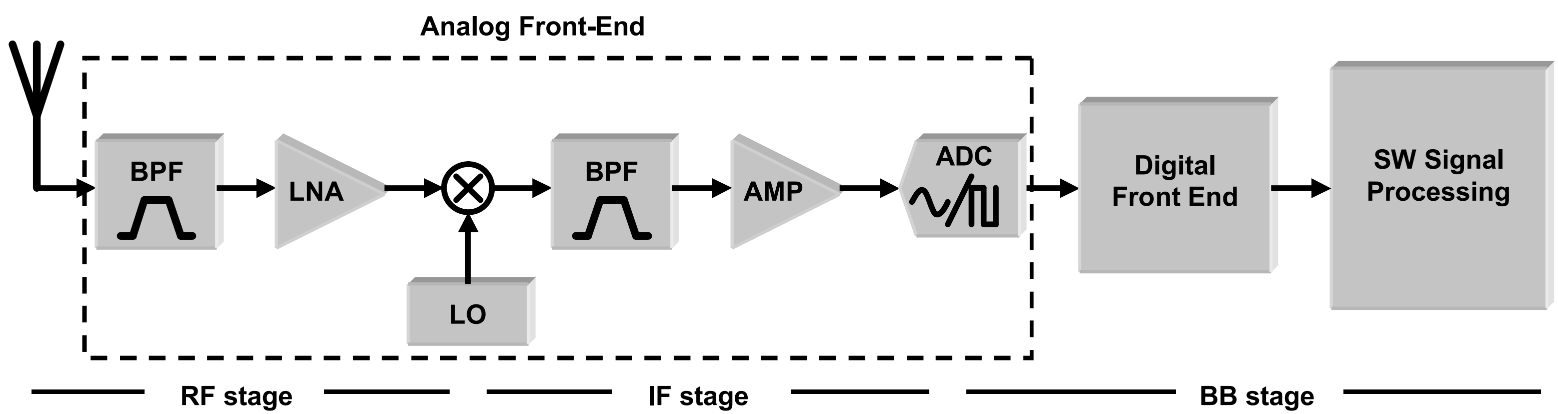
Ideal



Traditional

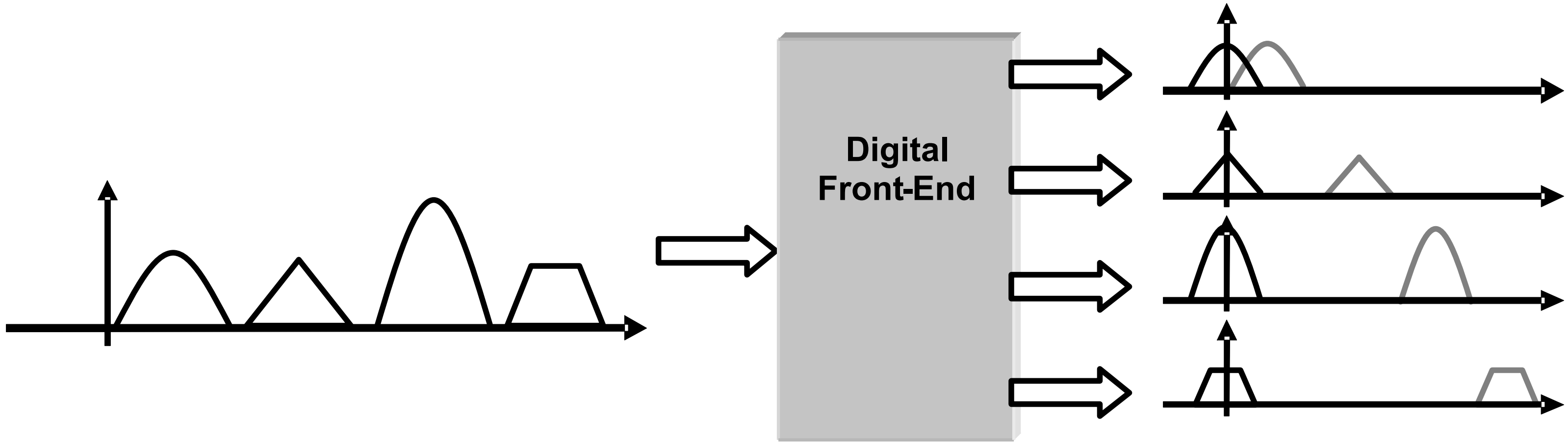


- Analog Front-End
- Digital Front-End
  - Reconfigurable components
  - Parametrizable components



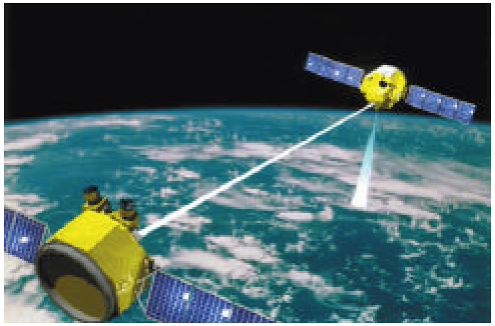
Channelization

- FDM – Frequency Division Multiplexing
- Multi-Channel Parallel Real-Time Channelization



Wideband SDR Channelizer Applications

- Civil
  - Base Stations
  - Comm. Sat.



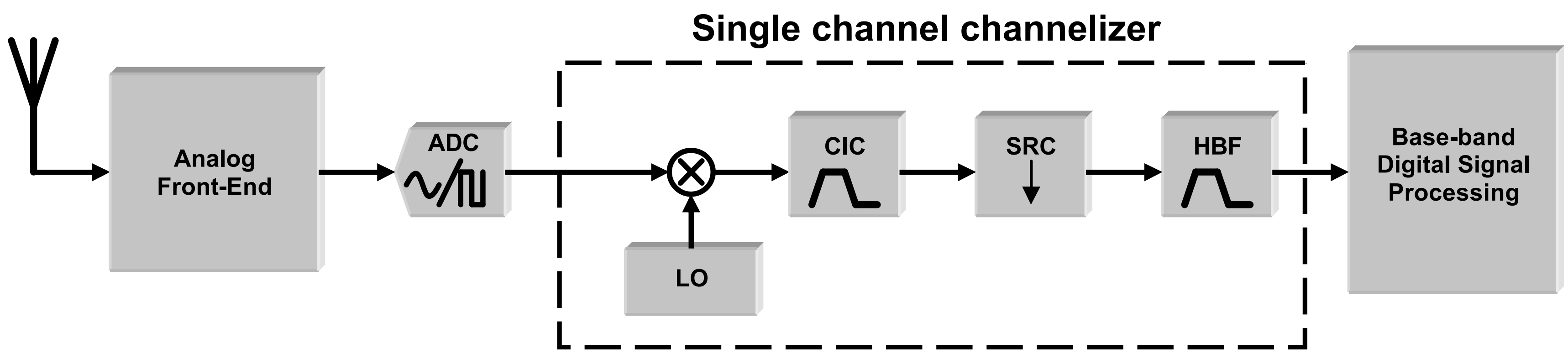
- Military
  - Coordination
  - Intelligence & Surveillance

Channelization Algorithms

- Traditional – Per Channel Approach
- Binary Tree Channelization
- Polyphase FFT Channelization

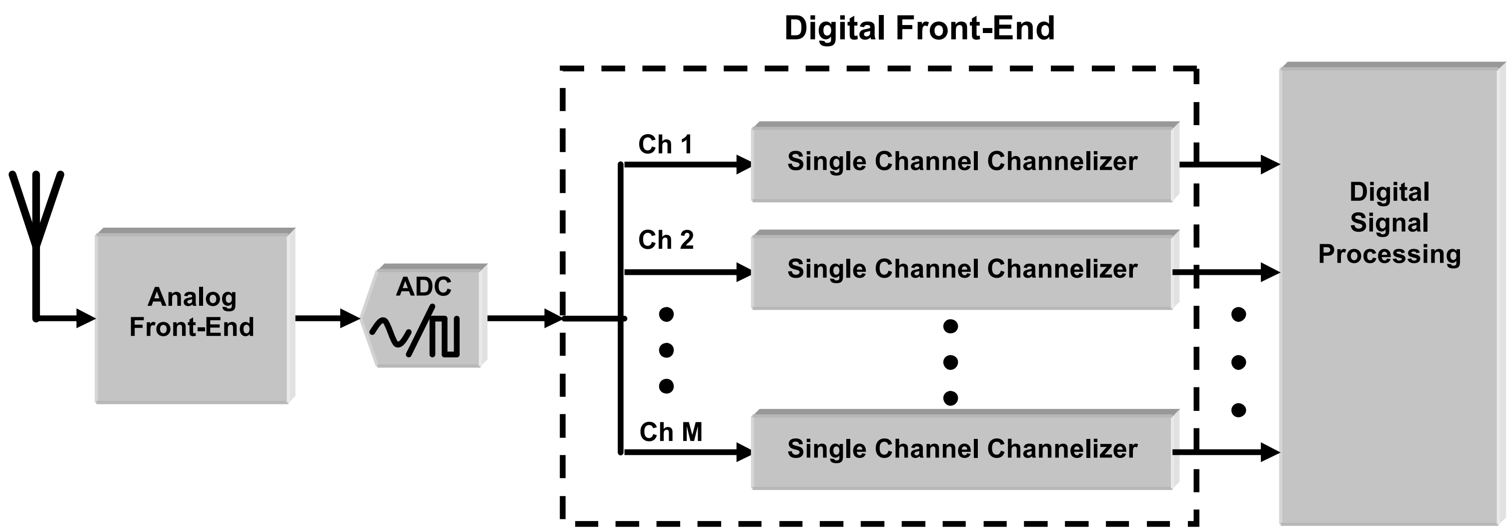
Per Channel Approach

- Single Channel Channelizer



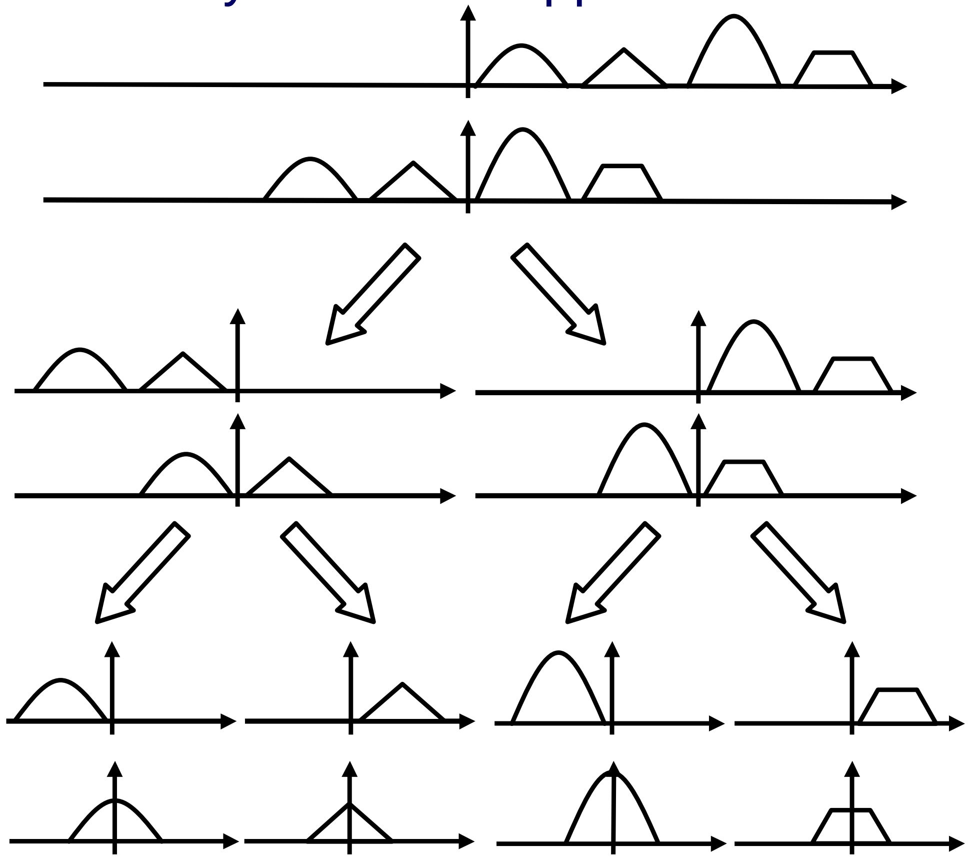
Per Channel Approach

- Stacked Single Channel Channelizers



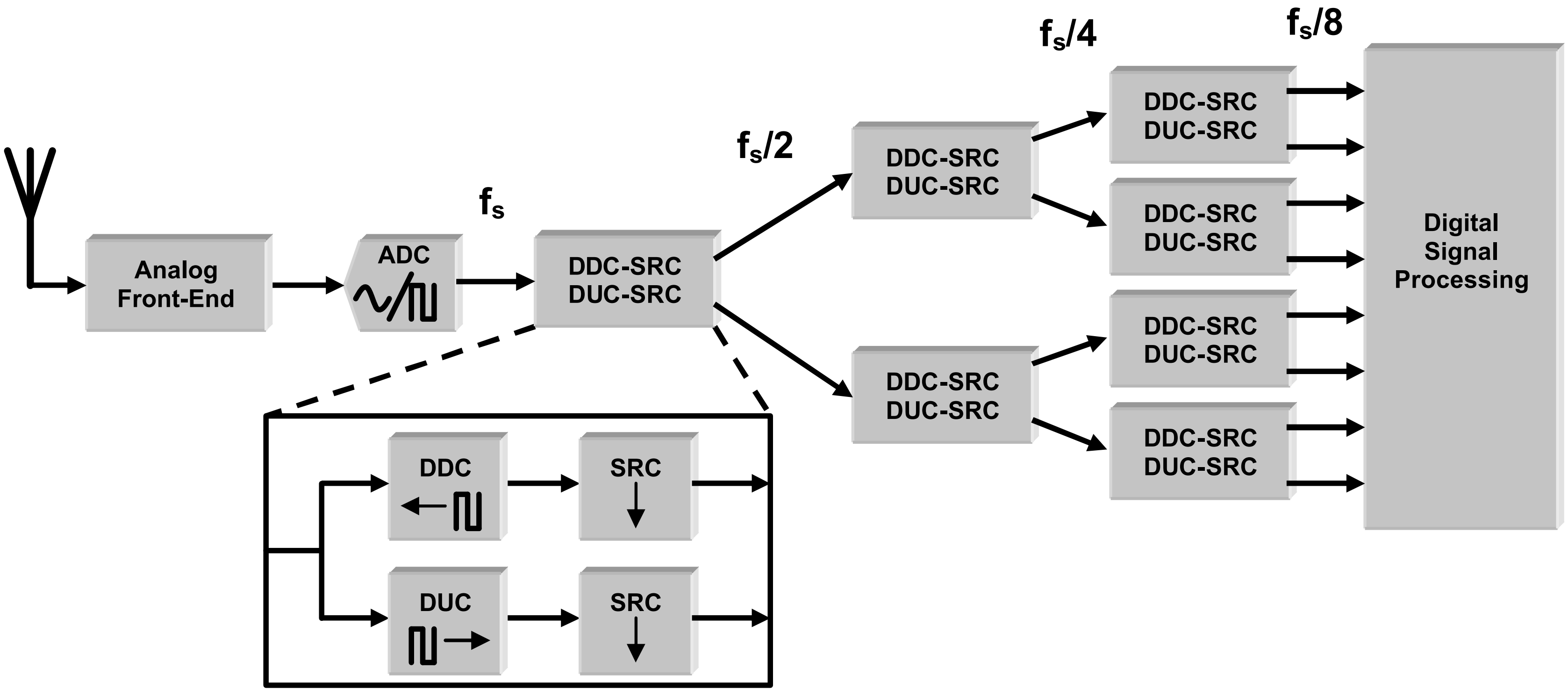
Binary Tree Channelization

- Spectrum recursively divided to upper and lower half bands.



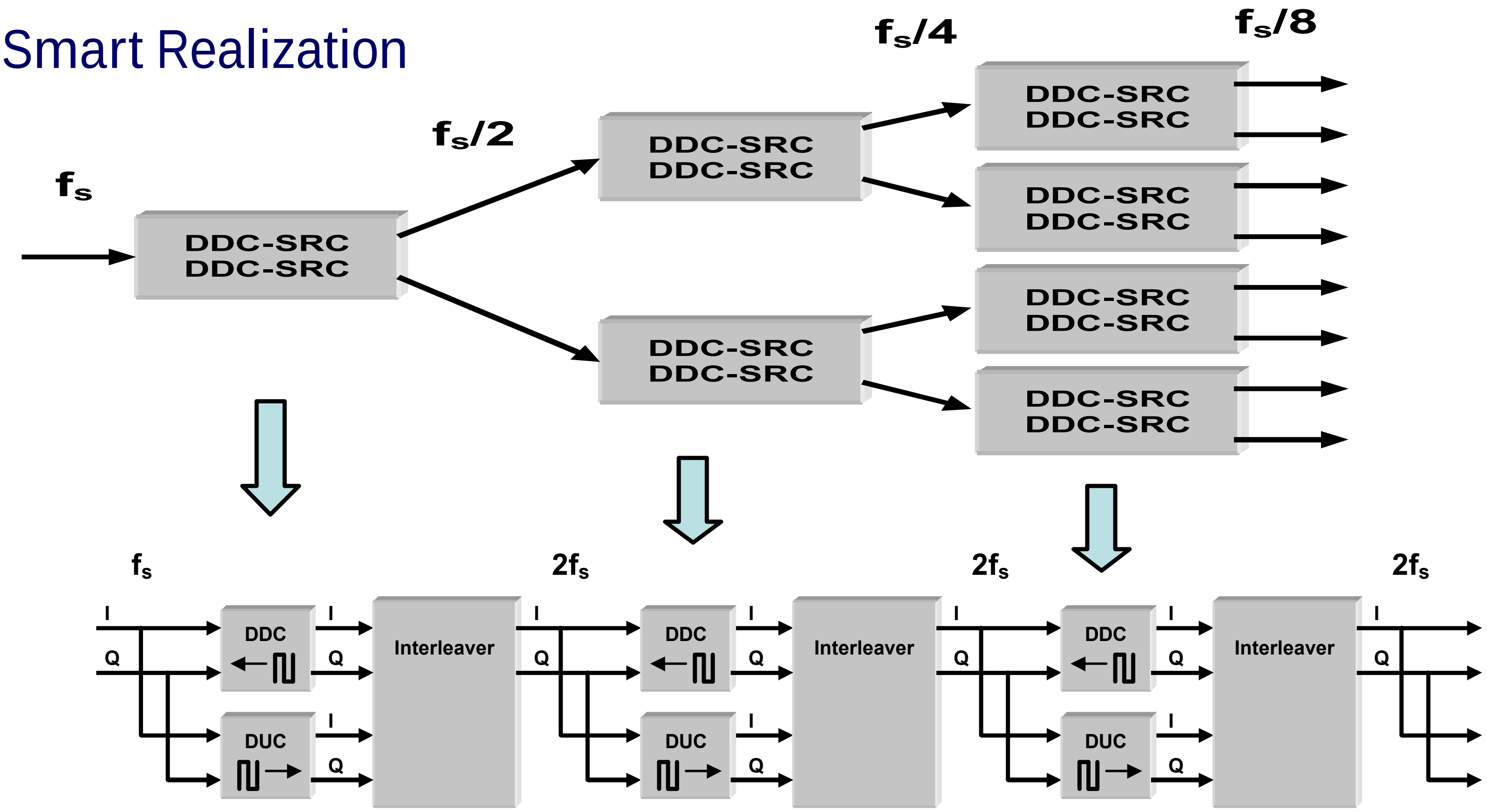
Binary Tree Channelization

- Structured as a binary tree



Binary Tree Channelization

- Smart Realization

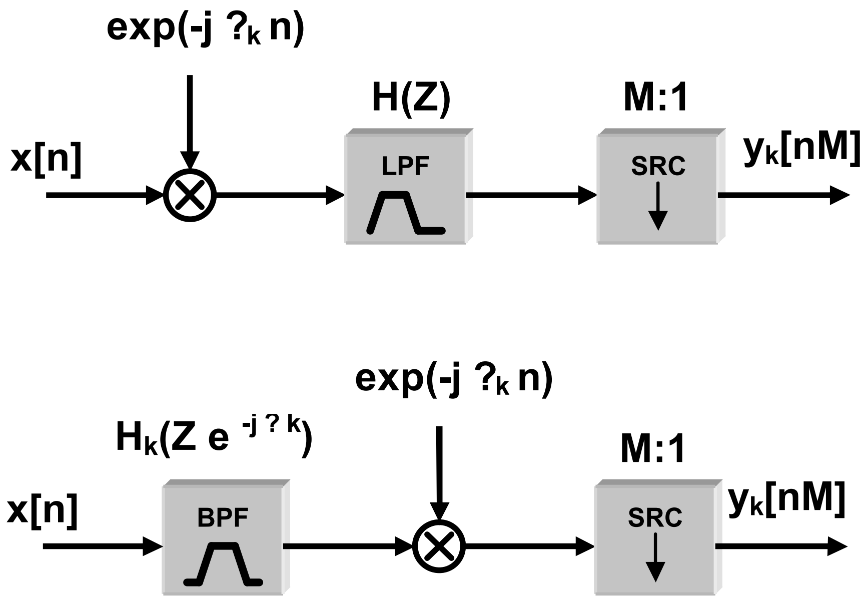


Polyphase FFT Channelizer

- Improvement of the per-channel approach.
- Considering overall sample-rate parameters.
- Exploiting FFT algorithm.

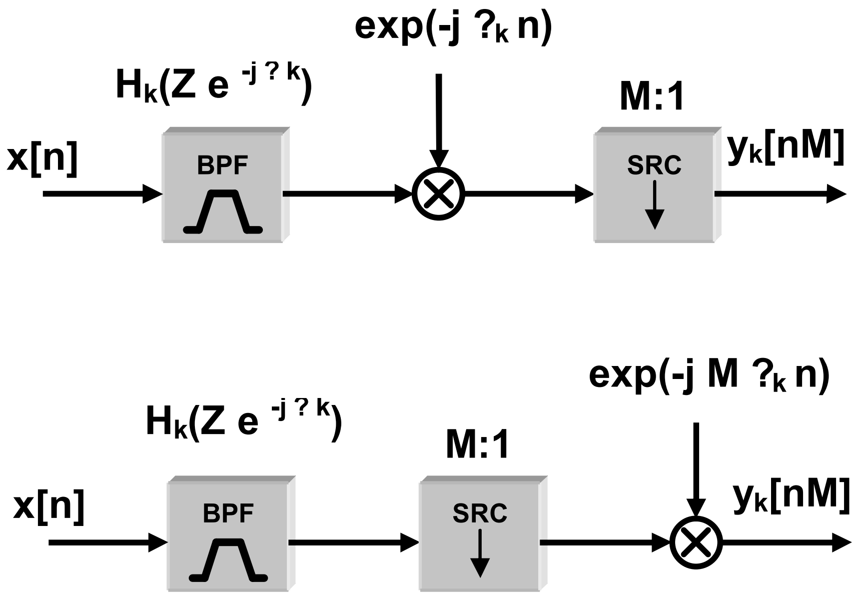
Polyphase FFT Channelizer

- Equivalence theorem: DDC + LPF = BPF + DDC



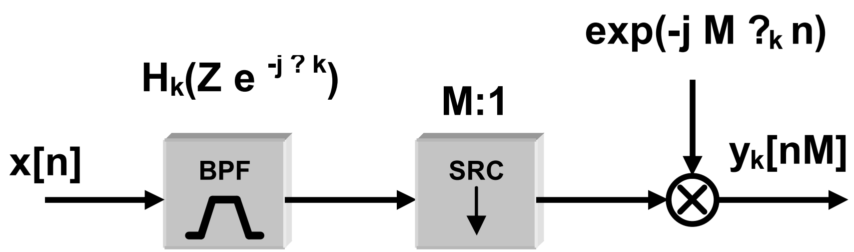
Polyphase FFT Channelizer

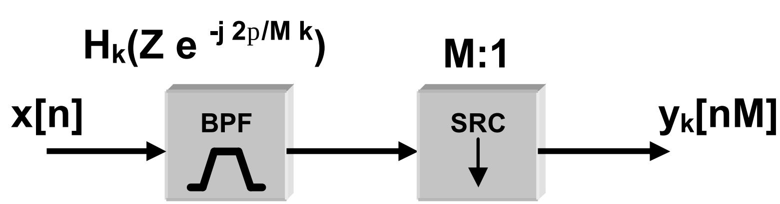
- Exploiting sample rate conversion



Polyphase FFT Channelizer

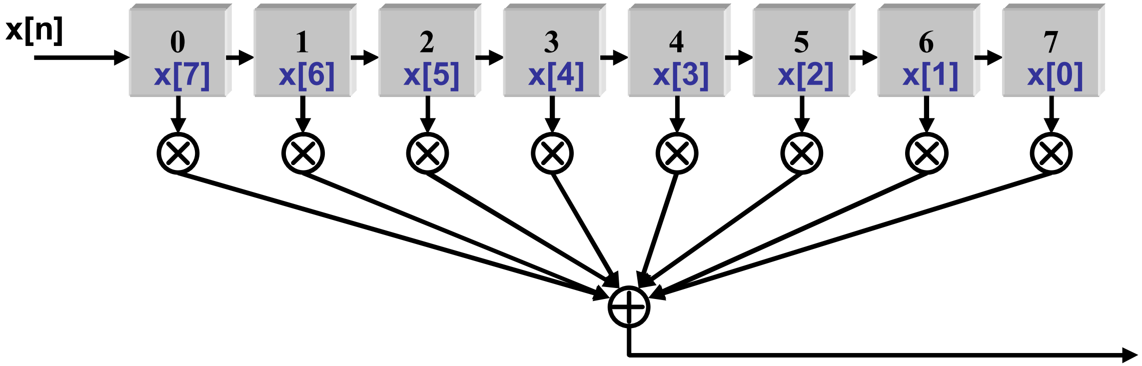
- k^{th} channel center frequency: $?_k = k\ 2p/M$



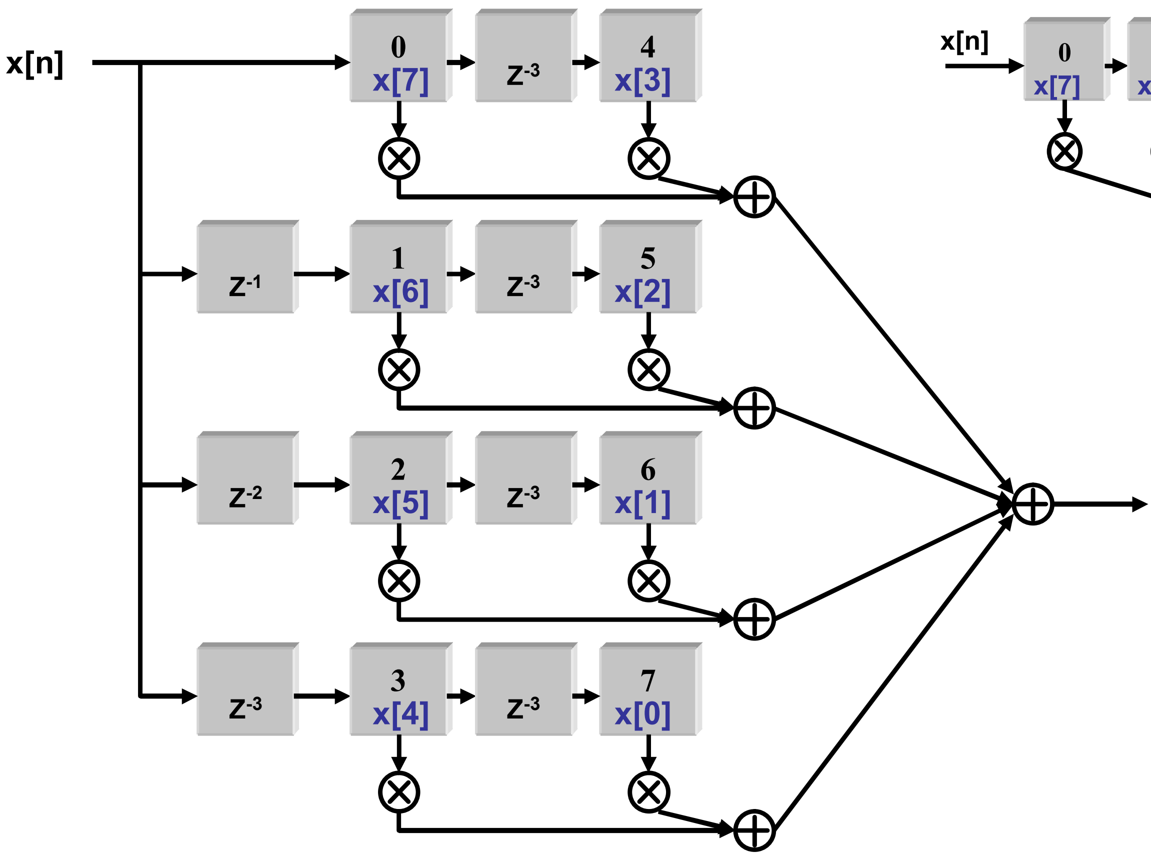


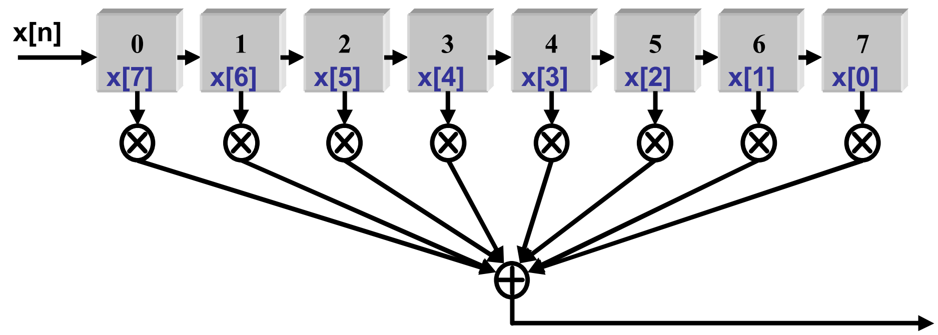
Constructing Filterbank

- Normal Filter



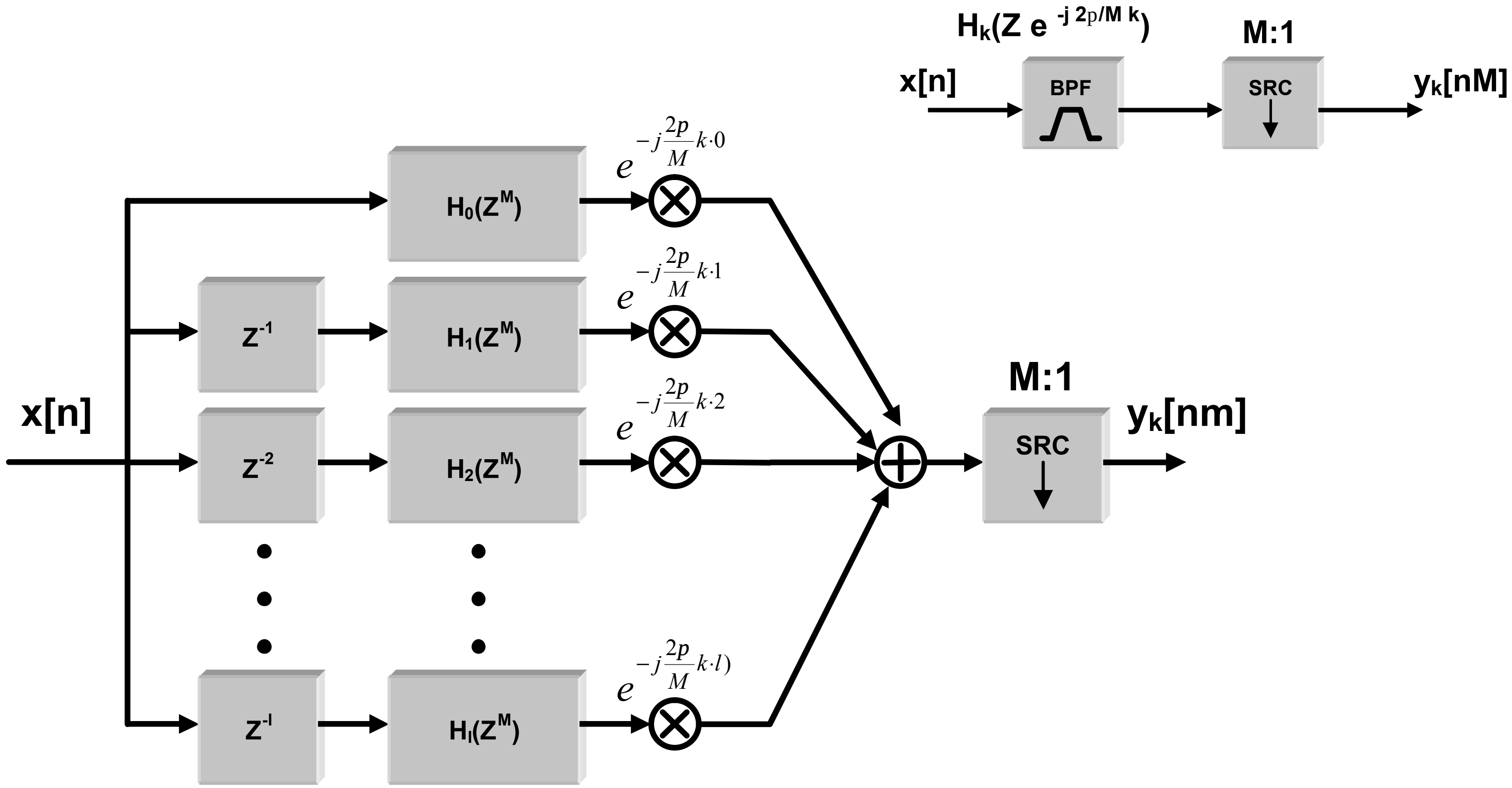
Decomposed Filterbank





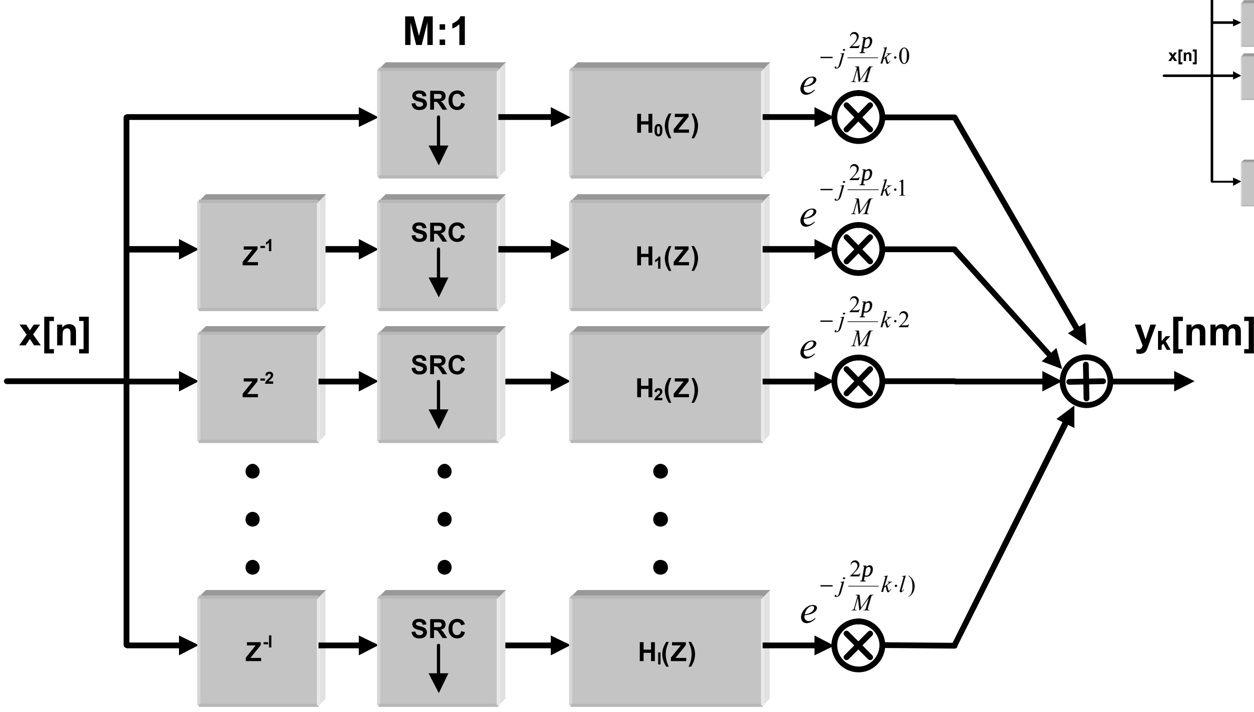
Polyphase FFT Channelizer

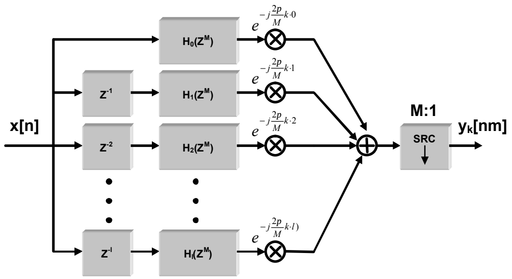
- Filterbank decomposition of the k^{th} Channel



Polyphase FFT Channelizer

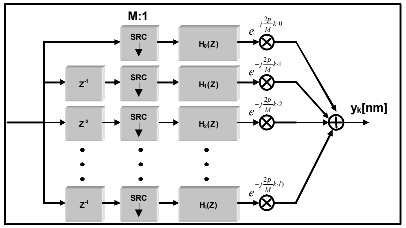
- Applying the noble identity on the the kth Channel

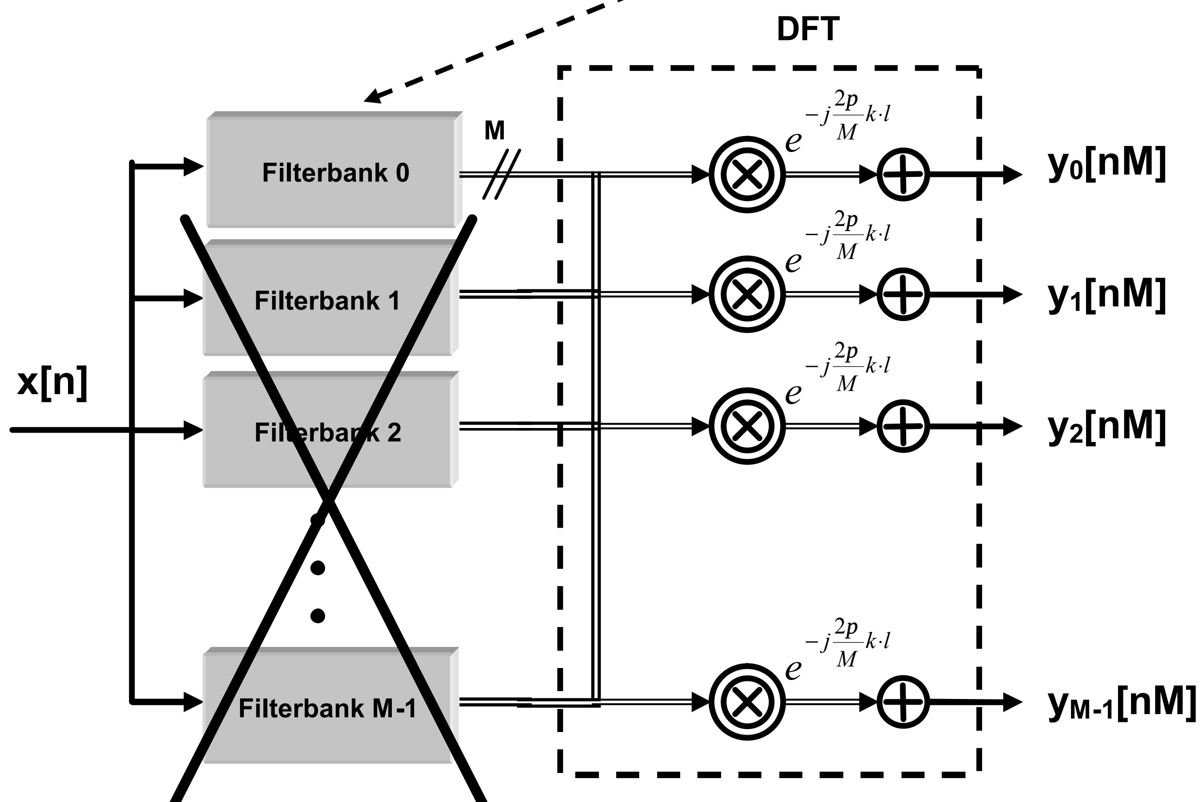




Polyphase FFT Channelizer

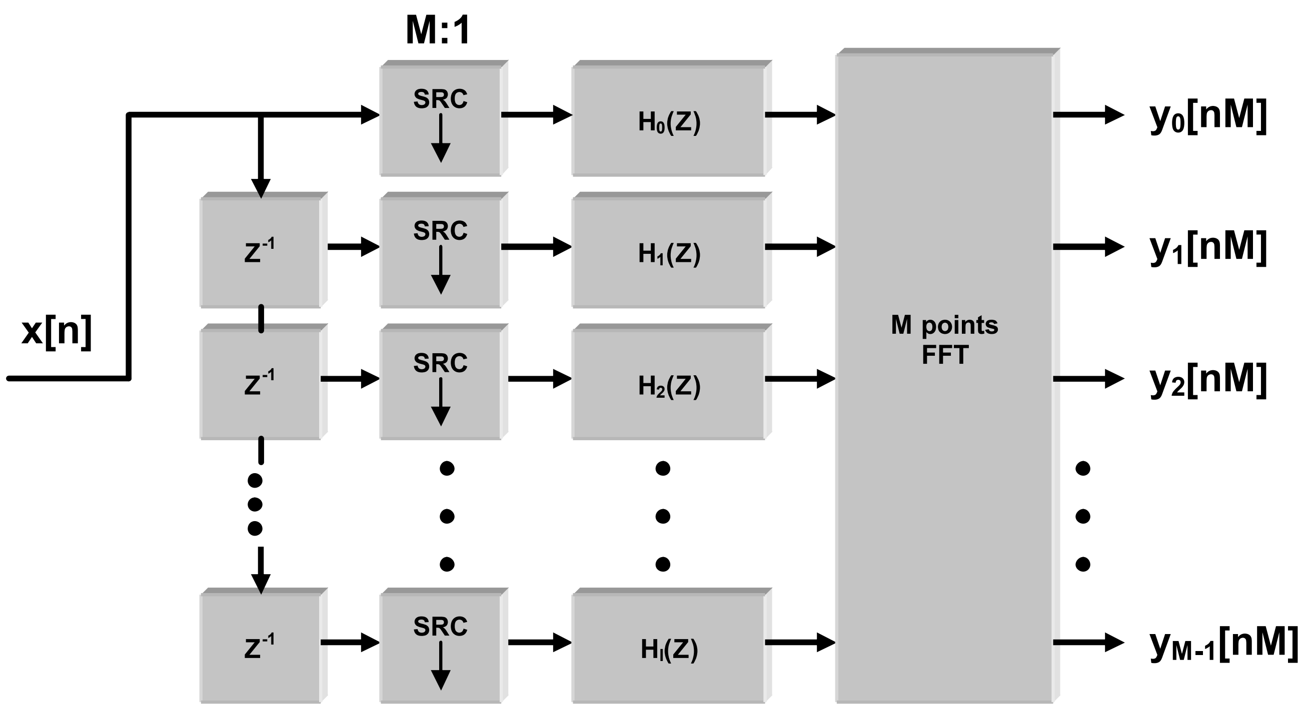
- Discarding M-1 filter-banks





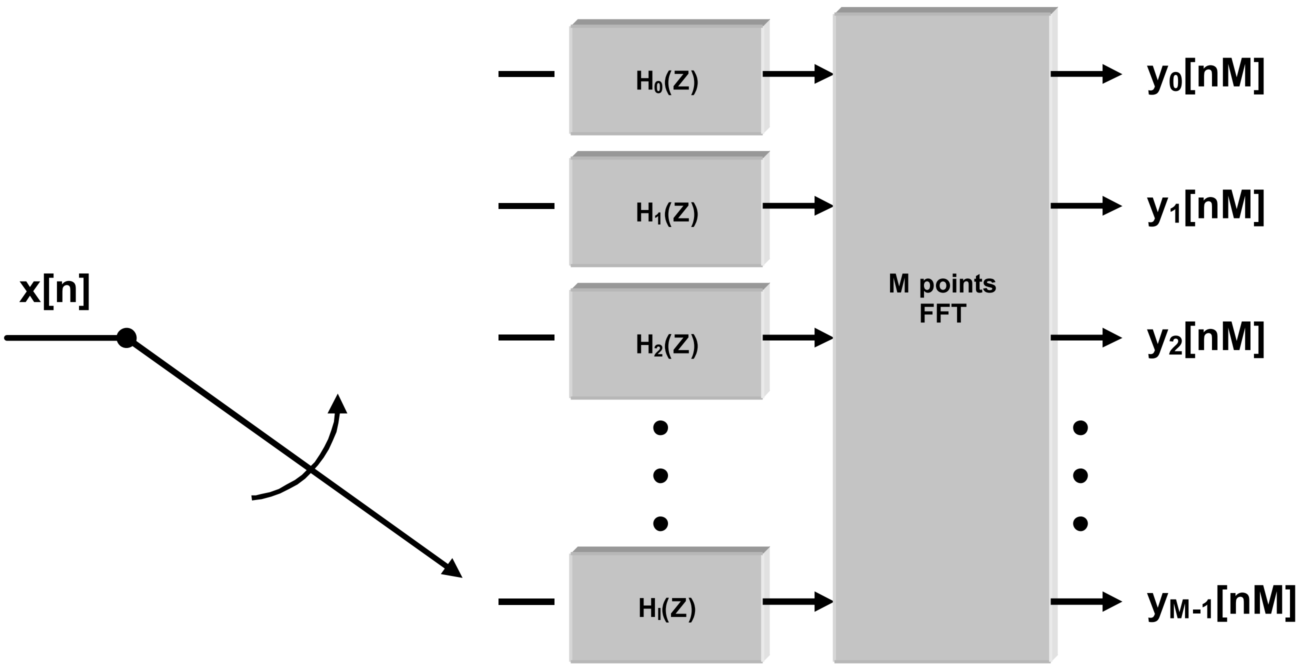
Polyphase FFT Channelizer

- Implementing the DFT using FFT



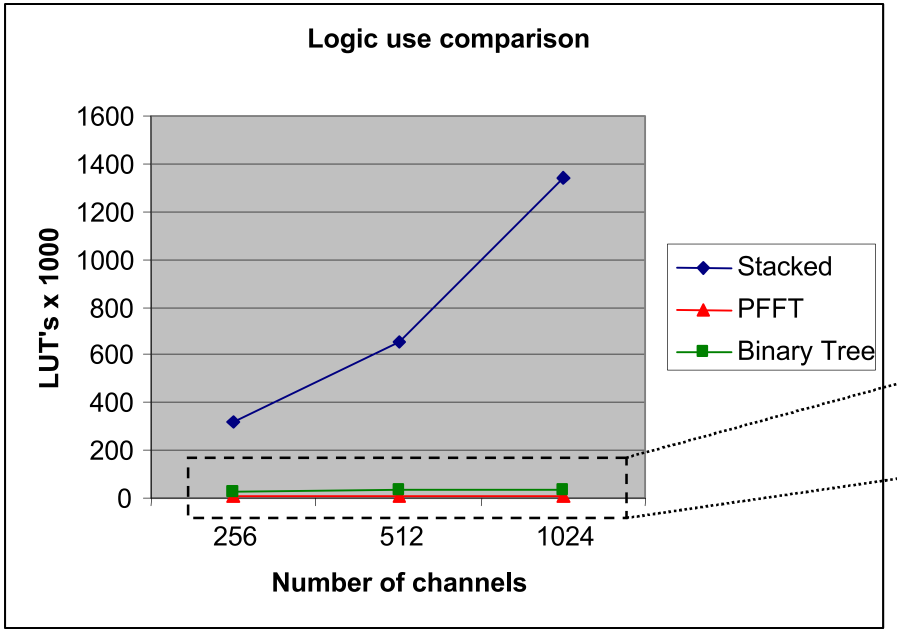
Polyphase FFT Channelizer

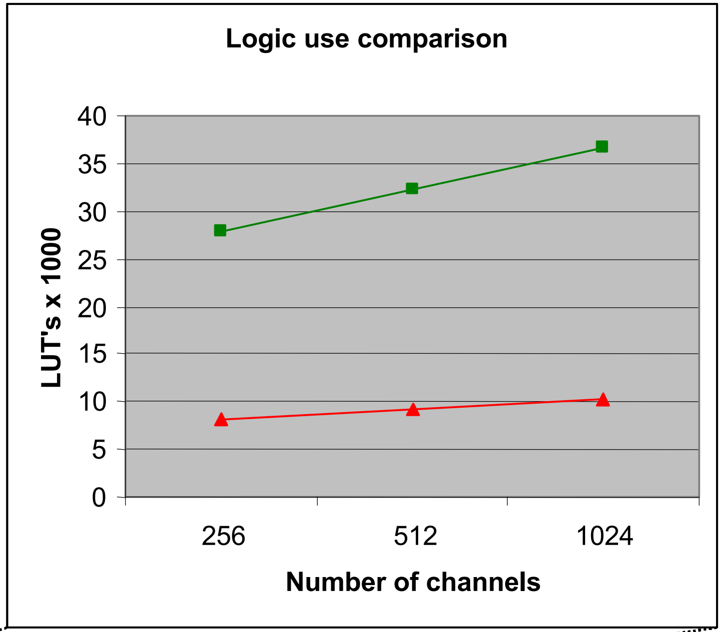
- Replacing the SRC's and delays by input commutator



Complexity Comparison

- Area utilization

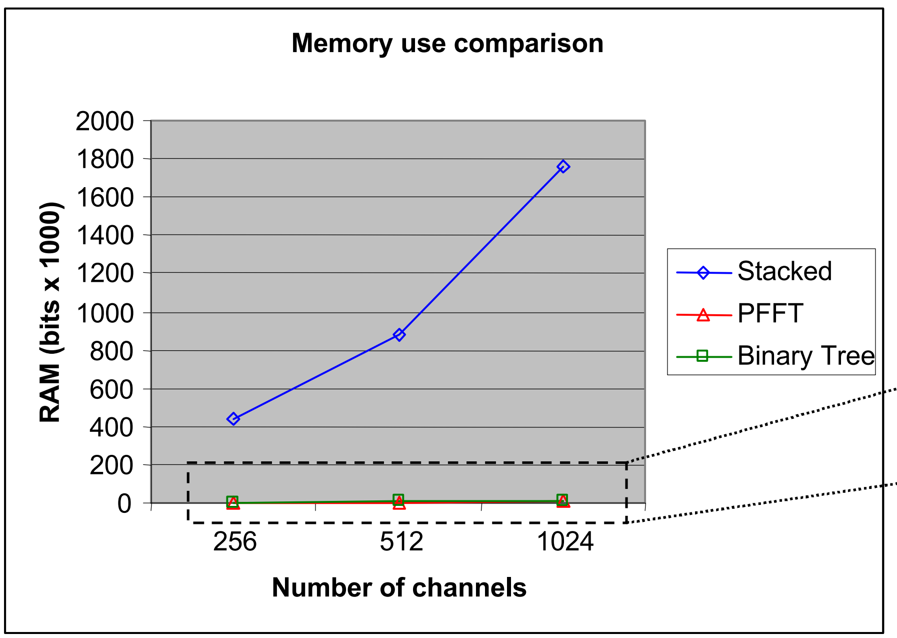


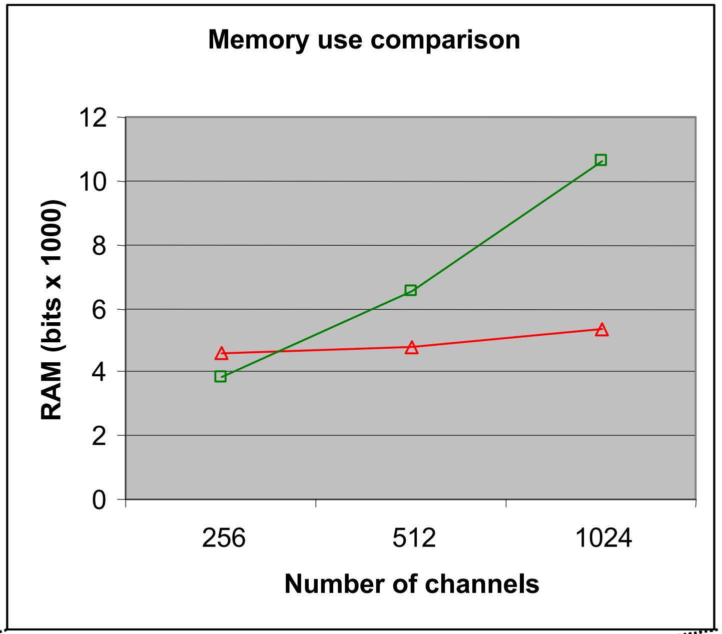


- PFFT has lowest Area utilization

Complexity Comparison

- Memory use





- PFFT has lowest Memory utilization for high number of channels

Qualitative Comparison

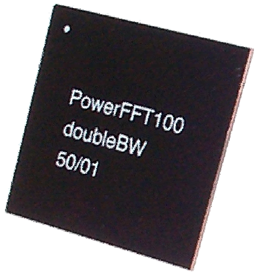
Aspect		Algorithm		
		Per-Channel	**Binary Tree**	**PFFT**
Computational Complexity for high number of channels		Poor	Good	**Excellent**
Silicon Cost Efficiency		Up to 3-20 channels	Up to 128-256 Channels	**Above 256 channels**
Group Delay		**Better**	Good	Good
Initial Design Flexibility:	**Independent channels**	**Yes**	No	No
	Number of channels	**Selectable**	2^{INT}	Preferably 2^{INT}
	Intermediate outputs	No	**Yes**	No
Flexibility for Reconfiguration:	**Addition / removal of channels**	**Excellent**	Poor	Poor
	Filtering performance adaptation	Poor	Poor	**Good**

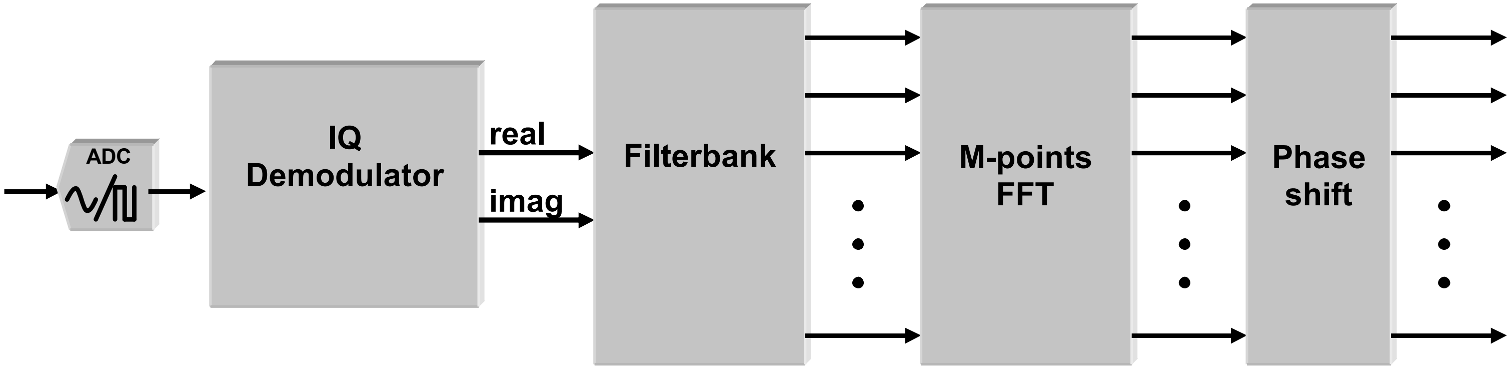
Comparison Conclusions

- Traditional algorithm is infeasible within the requirements
- The binary tree and the Polyphase FFT algorithms out performs the Stacked single-channel Channelizers algorithms
- The Polyphase FFT algorithm:
  - outperforms the binary tree algorithm for high nr. of channels
  - implementation is practical (low complexity)
  - is the chosen algorithm for implementing wideband receiver

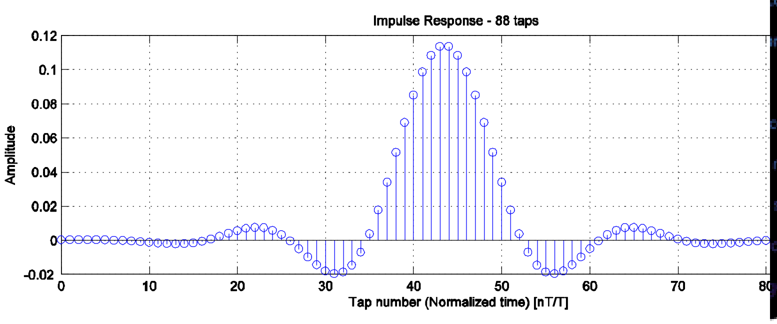
Polyphase FFT Wideband Channelizer Architecture (Current Work)

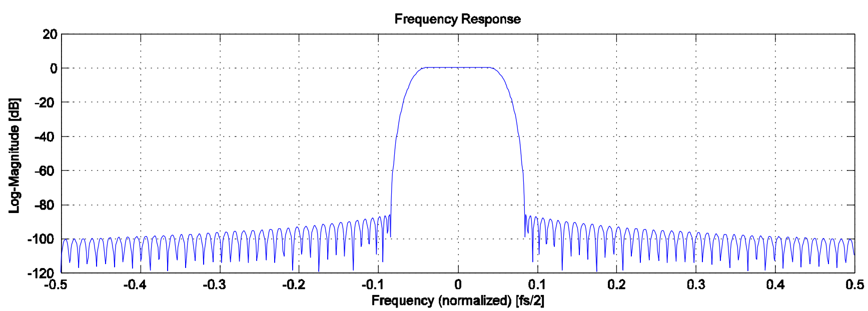
- A/D
- IQ-Demodulator
- Filterbank
- FFT coprocessor
- Phase correction

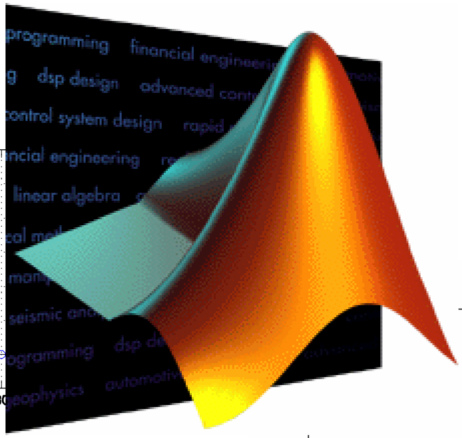


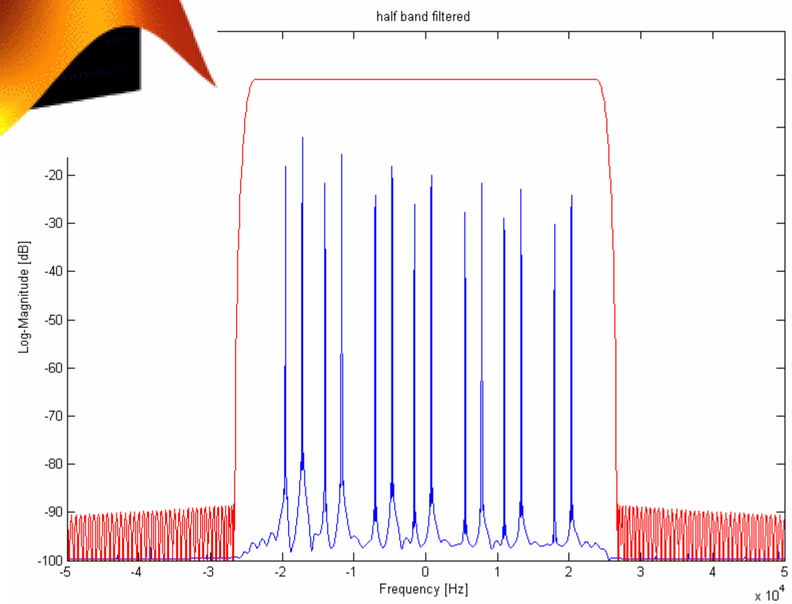


Matlab Model









The Horizon became
a Thousand Waves

Astrid Dahl