RF Engines Limited

Data Sheet

Pipelined Frequency Transform
PFT

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Date : 29 April 2002
Author : SJU
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Standard Pipelined Frequency Transform (PFT) Specification

Introduction

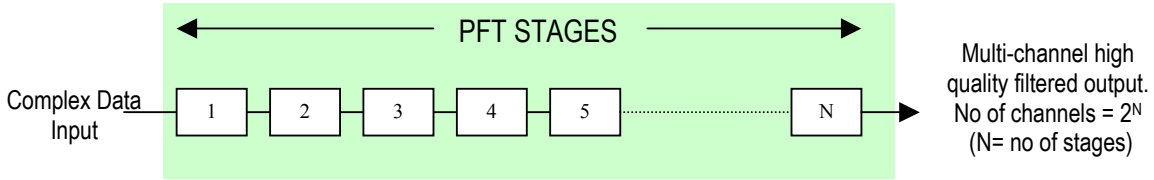
This data sheet describes a specific version of the RFEL Pipelined Frequency Transform (PFT), which has been implemented and tested in Xilinx Virtex E FPGAs. Comprehensive parameters are provided for this specific core and details are also given for a range of cores offered. Optional peripheral items and controls are detailed should they be relevant to your application. It is extremely important to note that the core architecture is very flexible and contains many factory parameterisable features. These features have been highlighted in the following information.

General Description

The Pipelined Frequency Transform is a proprietary, patent applied for, hardware design for implementation in FPGA or ASIC. It is a high specification multi-channel filter-bank optimised for real-time applications. This datasheet describes a particular configuration of a 10 stage 1024 point Xilinx Virtex E implementation. It is important to note that higher bit width and various filter parameters can be provided under contract. More information is available at www.rfel.com

The PFT should be considered as a superior replacement for an FFT, in filter bank applications, or as a multiple stack of digital down converters and filters. The core will accept a high sample rate complex input (up to 150Msps in Virtex II) and provide the individual filtered channel outputs at zero IF, I & Q in a multiplexed continuous stream for onward processing. The PFT is not a block processing system but a continuous pipelined process. An optional item in the core is a highly optimised Distributed Half Band Filter (DHBF) design for filtering and conversion of the real A/D input data down to the complex base-band format required for input to the PFT.

Figure 1. Basic PFT



Features

- Proven in Xilinx Virtex E, placed and routed in Virtex II and other FPGA devices.
- Programmable up to 10 stages (single Virtex FPGA), 4 to 1024 bin output (higher stages and concurrent stage outputs optional).
- Processes wide band signals (150MHz Spectrum Bandwidth) in continuous, **real time.**
- 8 bit real data input at up to **300Msps** (higher bit widths optional).
- 75dB stop band rejection filters (filters up to 130dB available).
- Minimal bin overlap, giving high signal definition.
- High performance and density guaranteed through optional Relationally Placed Macro (RPM) mapping and placement technology.
- Fully synchronous design.
- Flexible HDL design methodology.

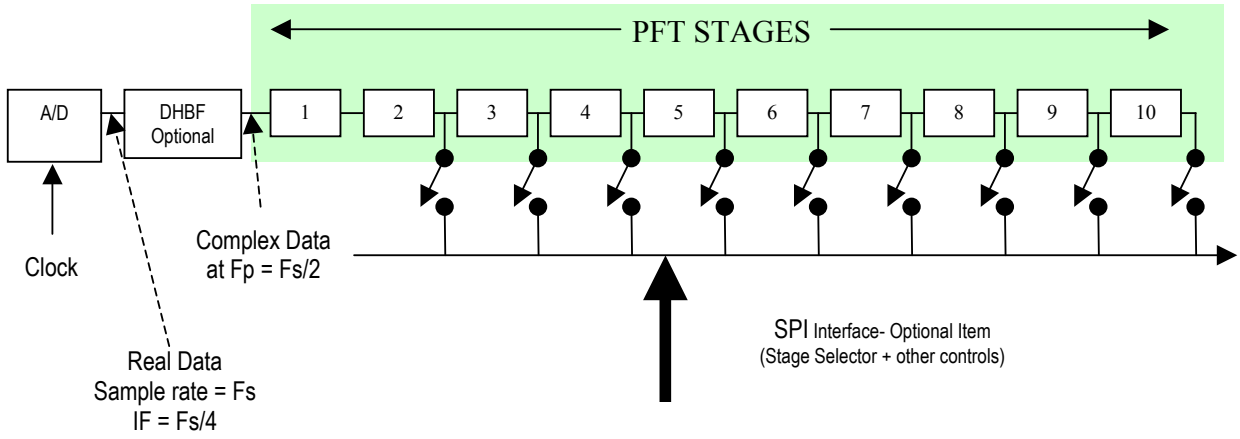
Applications

- FFT replacement – improves system performance for many systems currently using FFTs
- Digital down-converter replacement
- Multi-channel communications filtering
- Electronic warfare (radar, sonar, surveillance)
- Real time spectral analysis
- High specification filter bank
- OFDM systems

Functional Description

The input to the PFT is a complex data stream running at up to 150Msps in a Virtex FPGA. In this specific core a real data stream is first passed though an optional Fs/4 DHBF which down converts the input to a zero IF, base-band, complex I and Q signal. This requires that the real input signal is centred at an IF of +Fs/4 or any Nyquist interval that the A/D can accommodate. If the real data is not centred at an IF of Fs/4 and requires a complex down converter to achieve zero IF, RFEL can also provide a suitable core. The complex I & Q signal is then passed through the band splitting function of the PFT.

Figure 2. Functional Block Diagram (including peripheral optional items)



In Figure 2. above if we assume an A/D clock rate of 204.8MHz then the complex data rate out of the DHBF would be 102.4Msps (i.e. 102.4 MHz of spectrum bandwidth to be channelised). The filter response for the DHBF in this standard core is shown in Figure 3 below, (other designs of DHBF can be provided under contract). This complex data stream then passes through the PFT where it is band split in successive stages to produce a final output of 1024 channels. Using the example of a 102.4Msps complex input, the bin spacing would be 100kHz (102.4MHz/1024).

In this design the output of the core can be selected from the intermediate PFT stages by use of an optional Serial Peripheral Interface (SPI), this interface and its facilities are described later. Designs can be provided where simultaneous outputs from any number of stages are required. The individual PFT output bin filter shape used in this core is shown in Figure 4. Although the core uses FIR filters of this particular shape, almost any filter can be supplied to match specific application requirements, e.g. minimum phase or Gaussian. In this example the output sample rate of each individual bin is twice oversampled, producing a filter which is flat to the edge of the pass band with no aliases.

Figure 3. Half Band Filter shape (Standard PFT)

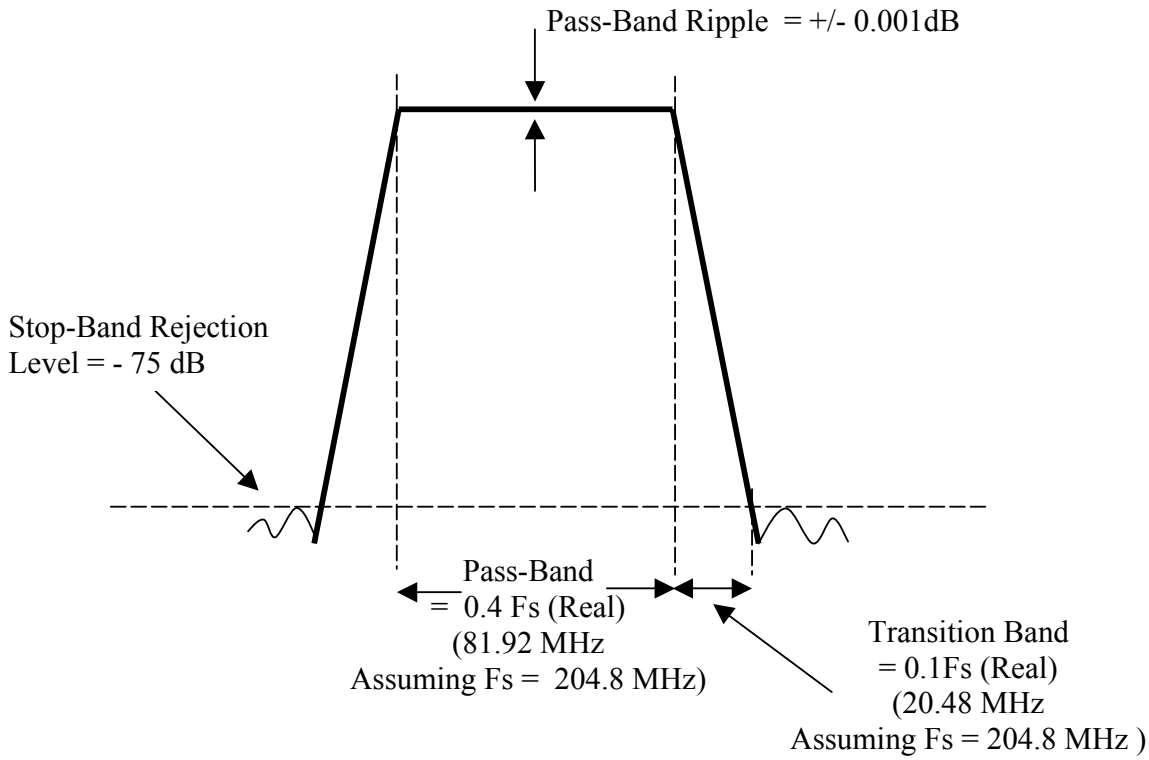
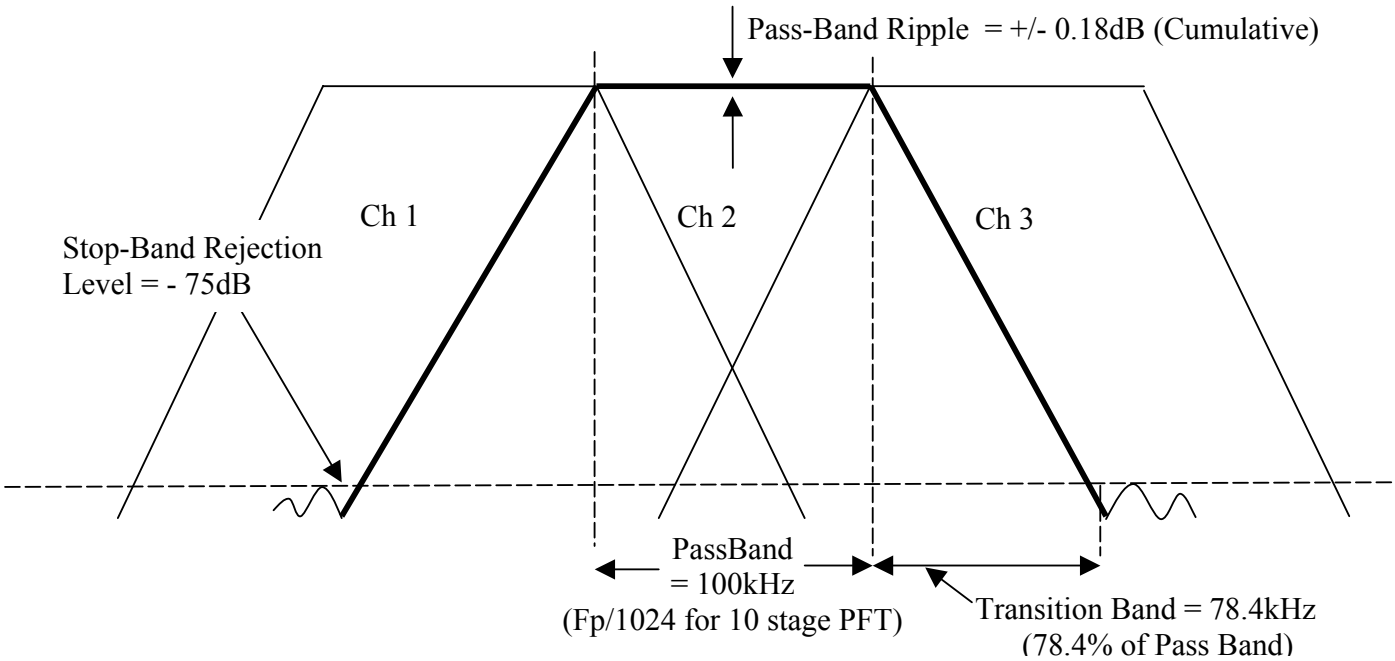


Figure 4. PFT Output Bin Filter Shape (Standard PFT)



Please note that in a simple weighted FFT the bin overlap will spread across several bins whereas in the PFT the bin overlap can be tailored to minimum levels by design. With a bin overlap of only 50% a CW signal will only ever appear in two bins, so that the signal detection resolution is massively improved.

Performance Specifications of Implemented Virtex E Design (See Annex A for other cores)

Parameter	Specification
Maximum input rate	256 Msps real via DHBF or 128 Msps complex direct into PFT stage 1.
Input bit width	8 Bit (higher bit width designs available)
Usable bandwidth	Centre 800 bins (approx for 1024 point 10 stage PFT. Depends on DHBF and front end RF design)
Bin resolution / spacing	Dependent on input data rate and number of stages selected. For example, for Fp (complex data rate at input to PFT) of 102.4 MHz and 6 stage PFT (64 bins) selected. Bin spacing = 102.4MHz/64 = 1.6MHz.
Dynamic range (spurious free)	75dB
Adjacent (bin) Channel Rejection	Standard system 17dB at centre of adjacent bin 75dB to other bins.
Filter (bin) selectivity (shape factor)	-60 to –3 dB bandwidth ratio = 1.64:1
Bin magnitude error (Ripple error)	+/-0.18dB (10 stage cumulative, less for earlier stages)
Group delay	Linear phase constant group delay.
Update rate per channel	System clock period x 512 i.e. 5uS with a system clock of 102.4 MHz.
Update rate per 1024-channel frame	System clock period x 512
Hardware delay (throughput latency)	10 clocks (Fp) per stage

These figures do not consider individual filter impulse responses. Please refer to the document “Transient Response White Paper “, available from RFEL’s web site http://www.rfel.com

Core Implementation Data Virtex E (4-chip RFEL demo system)

This implementation **includes the DHBF and SPI** interface functionality.

Supported Family	Device Tested	CLB Slices	Clock IOBs	IOBs	Performance* (Clk fmax)	Xilinx Tools	Special Features
VirtexE Chip 1	V1000E-6	8000	1	107	120 MHz	3.3 07i	12 Block RAMs, 1 DLL
VirtexE Chip 2	V1000E-6	9566	1	95	120 MHz	3.3 07i	20 Block RAMs, 1 DLL
VirtexE Chip 3	V1000E-6	8874	1	107	120 MHz	3.3 07i	12 Block RAMs, 1 DLL
VirtexE Chip 4	V1000E-6	9032	1	125	120 MHz	3.3 07i	16 Block RAMs, 1 DLL

*** 128 MHz for –7 speed grade chips**

This same standard PFT design with DHBF and SPI interface capability would also fit within a Virtex 3200 E (XCV3200E)

Please refer to Annex 'A' for various PFT implementations on Xilinx Devices.

IP Delivery Format.

Provided With Core	
Documentation	Specification \ Data Sheet, Testbench descriptions
Design Format	EDIF netlist or programming bitstream
Constraints File	UCF (user constraints file)
Verification	VHDL Testbench including ModelSim scripts, Test Data Files, VHDL functional simulation netlist (pre-compiled for ModelSim).
Instantiation Template	VHDL

Core Implementation Using Other Devices

This core is portable to other devices such as the Altera 'Apex' FPGAs.

Power Requirements

The power requirements for the core are highly dependent on the target device, size of implementation, and clock rate. RFEL can provide individual power estimates for a particular design where required.

Please note that RFEL have conducted tests with a semi-custom ASIC supplier where a VHDL design has been successfully synthesised for production. This test resulted in a reduction in power of around 75%.

PFT output format

The data output format of the PFT is 2 X 16bit signed integer I & Q serial data streams, odd bins in one channel and even bins in the other, bins are output in frequency order. Each data stream runs at the same clock rate (Fp) originally input to stage 1 of the PFT. This means that for every complex data sample going into stage 1 of the PFT engine, two data samples come out in the form of a complex value (I & Q) i.e. each bin output is twice over-sampled. RFEL can output the data in other configurations and formats, including IEEE floating point.

Figure 5. PFT Input/Output diagram

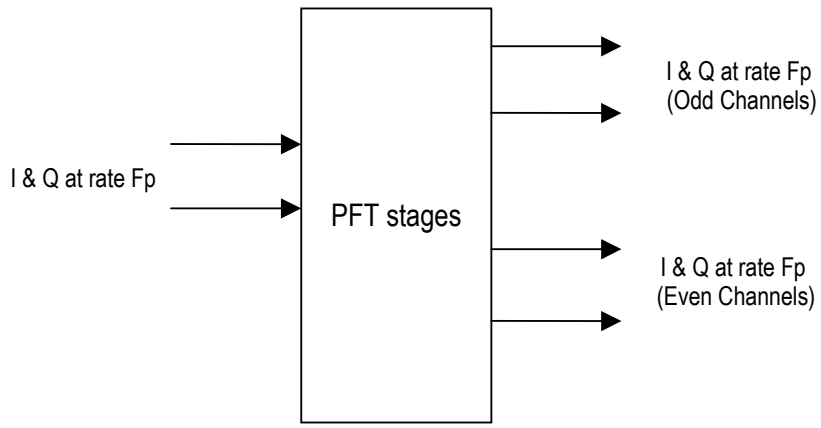
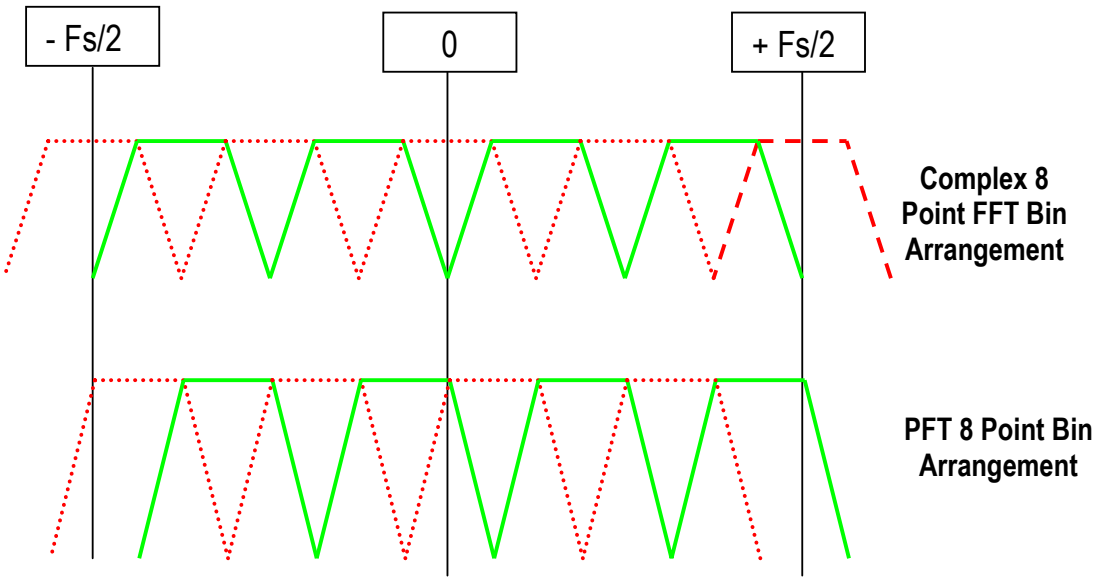


Figure 6. PFT bin format versus FFT bin format



Note that, unlike the FFT, PFT bins are symmetrically spaced either side of zero frequency and there is no bin centred on zero frequency. *In cases where an FFT-like frequency structure is required, a complex down-converter may be used at the input to the PFT, shifting the spectrum down by a frequency equivalent to one half bin at the PFT output.*

Also note that, like the FFT, not all bins will be usable. The bins cover the full Nyquist bandwidth of Fs/2 and, depending on the performance of the anti-aliasing filter (not shown but necessary in practice), the usable bandwidth will be typically Fs/2.56. Thus, for example, the output of a 10 stage PFT will contain 1024 bins (samples) but only the 800 centre bins are alias-free.

Interface Specification

Interface Specification (Standard Core)			
DHBF Signals			
Signal	**Format**	**Direction**	**Description**
OddIn(7:0)	STD Logic Vector	Input	De-multiplexed odd data from A/D, synchronised to clk
EvenIn(7:0)	STD Logic Vector	Input	De-multiplexed even data from A/D, synchronised to clk
Clk	STD Logic	Input	<102.4 MHz System clock (A/D clock/2)
Sync	STD Logic	Output	Active high pulse (1 clk pulse wide) Coincident with bin 0
IDataOut(7:0)	STD Logic Vector	Output	8 bit in-phase data, zero IF, synchronised to clk
QDataOut(7:0)	STD Logic Vector	Output	8 bit quadrature data, zero IF, synchronised to clk
PFT Signals			
IDataIn(7:0)	STD Logic Vector	Input	8 bit in-phase data, zero IF, synchronised to clk
QDataIn(7:0)	STD Logic Vector	Input	8 bit quadrature data, zero IF, synchronised to clk
Clk	STD Logic	Input	<102.4 MHz System clock (A/D clock/2)
Sync	STD Logic	Output	Active high pulse (1 clk pulse wide) Coincident with bin 0
IOddbins(13:0)	STD Logic Vector	Ouput	16 bit I data (odd bins 1,3,5….1023), synchronised to clk
QOddbins(13:0)	STD Logic Vector	Ouput	16 bit Q data (odd bins 1,3,5….1023), synchronised to clk
IEvenbins(13:0)	STD Logic Vector	Ouput	16 bit I data (even bins 0,2,4….1024), synchronised to clk
QEvenbins(13:0)	STD Logic Vector	Ouput	16 bit Qdata (even bins 0,2,4….1024), synchronised to clk

Pinout

Pinouts can be locked for whole chip solutions to suit customer requirements. In this case the design will be delivered in bit stream format.

Verification Methods

Extensive functional (pre-synthesis) and timing (post place and route) simulations have been performed using the ModelSim simulator. Simulation scenarios, (including data files) and the test benches used for design verification, are provided with the core.

Parameterisability

The architecture of the core has been designed so that many of the parameters can be modified relatively easily for a minimal non-recurring engineering charge. These changes include number of stages, bit widths and filter parameters. Also the Silicon usage for the designs can vary significantly depending on length of PFT, clock speed, bit widths and filter parameters. Your requirement may use significantly less Silicon than this standard design. Please refer to Annex 'A' for further information.

Using our extensive in-house system design experience, RF Engines provide a free initial consultancy service to analyse the specific filter bank requirements within a system environment. If you wish to make use of this service please send a brief email to sales@rfel.com outlining your requirements.

Optional SPI Control Interface and Functionality

The SPI interface also controls optional features available within the core, as follows:-

Decimator – as the PFT output is a continuous data stream running effectively at the same rate as the complex input, some applications cannot deal with all the data. The decimator facility can configure the PFT to output every Nth frame, which has the effect of slowing down the output data rate.

Bin Selector – the bin selector function allows just a single channel to be selected for output from the PFT (e.g. select channel 762 from the 1024 available).

Stage Selector - the stage selector determines which PFT stage output is available at the final output.

Threshold Detector – a threshold level across one bin or a number of bins may be set so that the PFT output will only be enabled when this threshold level is exceeded.

NOTE: All of the above facilities work independently or together in any combination.

The RFEL SPI Physical and Electrical Interface

This implementation is a version of the SPI Interface tailored to control the PFT cores. The Interface is asynchronous to the internal core and can work at any SCLK period up to 20MHz (faster rates may be possible, depending on the device used to implement the core and other system issues).

Note that Interfaces can be tailored to customer's requirements.

This version of the Interface maintains up to 32 internal 8-bit registers that can have multiple uses, depending on implementation.

The Interface uses 5 interface lines:-

SCLK – Serial clock
SYNCIO – Start data transfer pulse
CS – Chip select
SDIO – Serial data In
SDOUT – Serial data out (not used in this implementation)

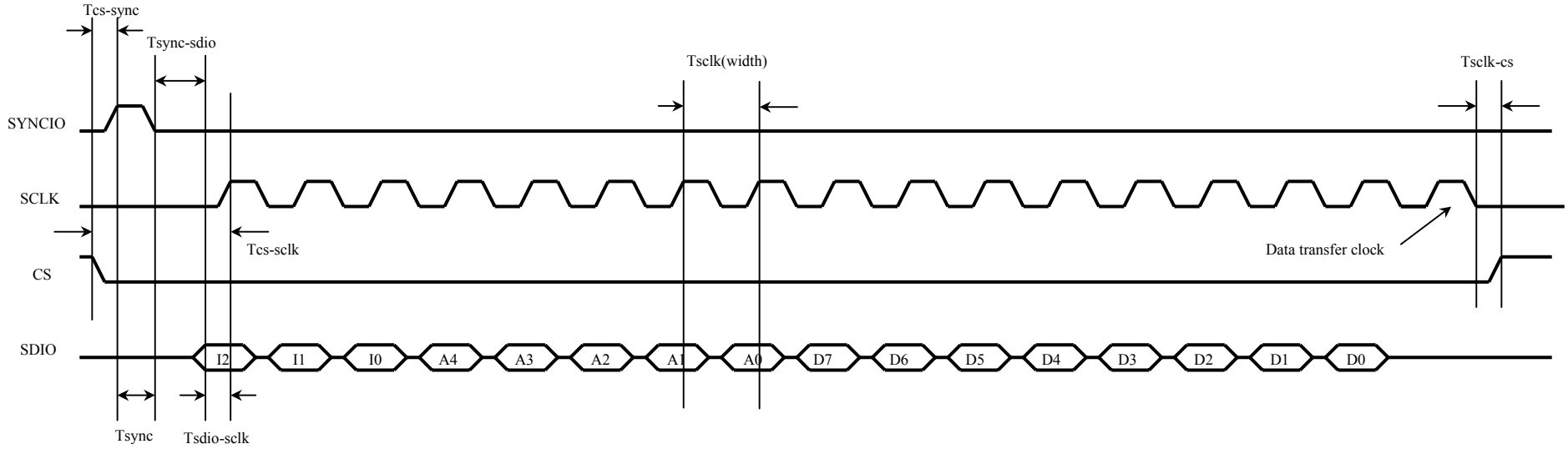
After the CS is taken low, the SYNCIO pulse is asserted to signal the start of data transfer. Serial data is clocked into the Interface on the rising edge of SDIO. The data must be presented as a 16-bit word formatted as Fig 7 and shifted into the SDIO port from left to right:-

Figure 7. Data Format

I2	I1	I0	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Description of the data word:
I2 – I0 = 3-bit Instruction word. Not used in this implementation. Set to 0.
A4 – A0 = destination register address of the following data.
D7 – D0 = data to write to the register.

Figure 8. RFEL SPI Interface Timing example



Symbol	Parameter	Min	Typ	Units
Tcs-sync	CS to SYNCIO setup time	0		ns
Tscyn-sdio	SYNCIO to SDIO setup time	0		ns
Tsync	SYNCIO pulse width	10	50	ns
Tsdio-sclk	SDIO to SCLK rising edge setup time	10		ns
Tcs-sclk	CS to first SCLK setup time	0		ns
Tsclk(width)	SCLK cycle width	20	50	ns
Tsclk-cs	Last SCLK to CS off time	0		ns

SPI Protocol

PFT SPI interface register map

Register	Description
0	Frame decimator 8 - Bit - skips number of frames set. 0 = off
1	Bits 7 to 0 = LSB for bin selector
2	Bits 2 to 0 = MSB for bin selector, bit 7 = '1' = bin selector on, '0' = off
3	Bits 7 to 0 = last PFT Stage number in chip for sync gen and bin select limiter.
4	If stage bypass implemented, Bit 0 = stage mux active = '1' Stage number is taken from register 3 above
5	Threshold detector - LSB for trigger offset (bits 7 to 0)
6	Threshold detector - MSB for trigger offset (bits 1 to 0) = 10 bits
7	Threshold detector - LSB for untrigger offset (bits 7 to 0)
8	Threshold detector - MSB for untrigger offset (bits 1 to 0) = 10 bits
9	Threshold detector - LSB for threshold level (bits 7 to 0)
10	Threshold detector - MSB for threshold level (bits 7 to 0) = 16 bits
11	Threshold detector - Bit 0 = control, '0' = off, '1' = on

How to Buy

The standard or modified cores are sold under an Application Licence. The price is normally made up of an up front payment followed by royalties. This pricing model is flexible to encompass single use implementations or large volume use. The Licence Agreement and quotations can be provided by contacting sales@rfel.com

Glossary

A/D	Analogue to Digital Converter
ASIC	Application Specific Integrated Circuit
CLB	Configurable Logic Block
DHBF	Distributed Half Band Filter
EDIF	Electronic Design Interchange Format
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
Fp	Complex Data Rate into PFT
FPGA	Field Programmable Gate Array
Fs	Real Data Rate into DHBF
HDL	Hardware Description Language
IF	Intermediate Frequency
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor Transistor Logic
LSB	Least significant bit
MSB	Most significant bit
PFT	Pipelined Frequency Transform
RFEL	RF Engines Limited
RPM	Relationally Placed Macro
SPI	Serial Peripheral Interface
UCF	User Constraints File
VHDL	Very High Speed Hardware Description Language

Annex 'A'
Core Implementations

Please read these notes before referring to tables below:

The tables below provide the worst-case Silicon usage for the PFT designs stated. RFEL have created these tables based on synthesis of the standard design presuming a total FPGA solution is required. The following factors should be considered and will most certainly reduce the Silicon usage significantly.

External memory

The tables below assume a total FPGA solution with no external memory. However, as the PFT length increases, its memory use grows at a faster rate than the logic requirement. Therefore it is possible to use smaller FPGAs with external memory, as used in the RFEL Virtex II cPCI card.

Complex Sample Rate

If the complex sample rate is significantly less than indicated, a different architecture can be used that will significantly reduce the Silicon requirements. The actual core speed will generally be controlled by the analogue to digital (A/D) converter device chosen. However, since all the cores specified will work at the 128MHz complex rate (150MHz in Virtex II), this may allow for several A/D outputs to be multiplexed through one core. RFEL have already provided designs that use this multiplexed feature**.**

Simultaneous Outputs

If simultaneous outputs are not required, or only required from a few selected PFT stages, again, the Silicon usage may be reduced.

Filter shape

The filter designs in the tables use very good quality shapes in terms of overlap, ripple and stop-band rejection. Any relaxation in these specifications will reduce Silicon requirements.

Conclusion

Silicon usage of the PFT is highly dependent on the actual configuration. Whilst the usage figures in these tables are worst case they can be reduced significantly by changes in the above-mentioned factors. To obtain a Silicon usage estimate more closely matched to your requirements please contact RFEL.

The tables below illustrate the Silicon usage for a selection of data widths, percentage overlap and ripple:-

8 BIT DATA

Stop band figure = dBc. Ripple Figure = +/- dBc

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	75	0.1	35	5.2	34	2%
7 (128 bins)	60dB	75	0.1	43	12.0	41	4.8
8 (256 bins)	60dB	75	0.1	51	25.4	49	9.7
9 (512 bins)	60dB	75	0.1	79	28.8	58	19.4
10 (1024 bins)	60dB	75	0.1	88	86.5	66	38.2
11 (2048 bins)	60dB	75	0.1	98	211.5	76	78.4

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	75	0.5	28	3.8	27	2
7 (128 bins)	60dB	75	0.5	35	9.1	33	4.1
8 (256 bins)	60dB	75	0.5	41	19.7	40	7.6
9 (512 bins)	60dB	75	0.5	63	23	46	15.2
10 (1024 bins)	60dB	75	0.5	70	69.2	53	30.5
11 (2048 bins)	60dB	75	0.5	78	169.2	61	63.1

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	50	0.1	49	7.6	47	2.78
7 (128 bins)	60dB	50	0.1	60	17.3	58	6.25
8 (256 bins)	60dB	50	0.1	71	36.0	69	12.5
9 (512 bins)	60dB	50	0.1	84	76.4	81	25.6
10 (1024 bins)	60dB	50	0.1	96	157.2	92	52
11 (2048 bins)	60dB	50	0.1	110	332.2	105	108.3

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	50	0.5	42	6.7	40	2.78
7 (128 bins)	60dB	50	0.5	52	14.9	50	5.56
8 (256 bins)	60dB	50	0.5	61	30.7	59	11.1
9 (512 bins)	60dB	50	0.5	72	65.3	69	22.2
10 (1024 bins)	60dB	50	0.5	83	134.6	79	44.4
11 (2048 bins)	60dB	50	0.5	94	284.6	90	93.0

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	75	0.1	38	5.2	39	1.39
7 (128 bins)	75dB	75	0.1	47	12.9	48	4.1
8 (256 bins)	75dB	75	0.1	56	27.8	56	9
9 (512 bins)	75dB	75	0.1	87	31.7	66	19.4
10 (1024 bins)	75dB	75	0.1	97	95.1	75	40.2
11 (2048 bins)	75dB	75	0.1	107	232.6	85	84.7

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	75	0.5	32	4.3	31	1.39
7 (128 bins)	75dB	75	0.5	39	10.5	38	3.4
8 (256 bins)	75dB	75	0.5	54	12	45	7.6
9 (512 bins)	75dB	75	0.5	62	37.9	53	15.9
10 (1024 bins)	75dB	75	0.5	70	89.9	61	32.6
11 (2048 bins)	75dB	75	0.5	79	202.4	69	68.7

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	50	0.1	55	8.65	53	4.1
7 (128 bins)	75dB	50	0.1	68	19.2	66	7.6
8 (256 bins)	75dB	50	0.1	81	40.3	78	14.5
9 (512 bins)	75dB	50	0.1	96	86.5	92	29.8
10 (1024 bins)	75dB	50	0.1	110	178.8	106	59.7
11 (2048 bins)	75dB	50	0.1	125	378.8	120	124.3

	PFT input of 8 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	50	0.5	49	7.6	47	2.7
7 (128 bins)	75dB	50	0.5	60	17.3	58	6.2
8 (256 bins)	75dB	50	0.5	71	36.0	69	12.5
9 (512 bins)	75dB	50	0.5	84	76.4	81	25.6
10 (1024 bins)	75dB	50	0.5	96	157.2	92	52.0
11 (2048 bins)	75dB	50	0.5	110	332.2	105	108.3

10 BIT DATA

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	75	0.1	42	6.7	41	2.78
7 (128 bins)	60dB	75	0.1	52	14.9	50	5.56
8 (256 bins)	60dB	75	0.1	62	30.7	59	11.11
9 (512 bins)	60dB	75	0.1	72	64.4	69	22.22
10 (1024 bins)	60dB	75	0.1	82	131.7	79	44.44
11 (2048 bins)	60dB	75	0.1	93	275.9	90	90.97

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	75	0.5	34	4.3	33	2.08
7 (128 bins)	60dB	75	0.5	42	10.5	40	4.17
8 (256 bins)	60dB	75	0.5	59	12.5	48	8.3
9 (512 bins)	60dB	75	0.5	67	39.4	56	17.3
10 (1024 bins)	60dB	75	0.5	75	93.2	64	34.7
11 (2048 bins)	60dB	75	0.5	84	208.6	72	72.2

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	50	0.1	59	9.6	58	3.4
7 (128 bins)	60dB	50	0.1	72	20.6	71	7.6
8 (256 bins)	60dB	50	0.1	86	42.7	84	15.2
9 (512 bins)	60dB	50	0.1	100	89.9	97	30.5
10 (1024 bins)	60dB	50	0.1	115	184.1	111	61.1
11 (2048 bins)	60dB	50	0.1	130	386.0	126	126.3

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	60dB	50	0.5	51	8.17	49	2.78
7 (128 bins)	60dB	50	0.5	62	17.7	60	6.25
8 (256 bins)	60dB	50	0.5	74	36.5	71	12.5
9 (512 bins)	60dB	50	0.5	86	76.9	83	25.6
10 (1024 bins)	60dB	50	0.5	99	157.6	95	52.0
11 (2048 bins)	60dB	50	0.5	112	330.7	108	107.6

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	75	0.1	47	7.6	45	2.78
7 (128 bins)	75dB	75	0.1	57	16.3	55	5.56
8 (256 bins)	75dB	75	0.1	68	33.6	65	11.11
9 (512 bins)	75dB	75	0.1	79	70.7	76	23.61
10 (1024 bins)	75dB	75	0.1	90	144.7	87	47.9
11 (2048 bins)	75dB	75	0.1	103	303.3	99	99.3

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	75	0.5	38	5.3	37	2.08
7 (128 bins)	75dB	75	0.5	47	12.5	45	4.86
8 (256 bins)	75dB	75	0.5	56	26.9	53	9.72
9 (512 bins)	75dB	75	0.5	86	30.2	62	19.44
10 (1024 bins)	75dB	75	0.5	95	90.8	71	38.89
11 (2048 bins)	75dB	75	0.5	105	220.6	81	80.56

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	50	0.1	67	10.10	65	4.17
7 (128 bins)	75dB	50	0.1	83	22.6	79	8.33
8 (256 bins)	75dB	50	0.1	98	47.6	94	16.6
9 (512 bins)	75dB	50	0.1	115	101.4	110	34.0
10 (1024 bins)	75dB	50	0.1	131	209.1	126	68.7
11 (2048 bins)	75dB	50	0.1	149	439.9	143	143.0

	PFT input of 10 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	75dB	50	0.5	59	9.6	58	3.4
7 (128 bins)	75dB	50	0.5	72	20.6	71	7.6
8 (256 bins)	75dB	50	0.5	86	42.7	84	15.2
9 (512 bins)	75dB	50	0.5	100	89.9	97	30.5
10 (1024 bins)	75dB	50	0.5	115	184.1	111	61.1
11 (2048 bins)	75dB	50	0.5	130	386.0	126	126.3

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	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	75	0.1	55	8.6	53	4.17
7 (128 bins)	85dB	75	0.1	67	18.7	64	7.64
8 (256 bins)	85dB	75	0.1	79	38.9	76	14.5
9 (512 bins)	85dB	75	0.1	92	81.2	89	28.4
10 (1024 bins)	85dB	75	0.1	105	165.8	101	56.2
11 (2048 bins)	85dB	75	0.1	119	345.6	114	114.5

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	75	0.5	50	8.17	48	2.78
7 (128 bins)	85dB	75	0.5	61	17.3	59	6.25
8 (256 bins)	85dB	75	0.5	72	35.5	69	12.5
9 (512 bins)	85dB	75	0.5	84	74.0	81	25
10 (1024 bins)	85dB	75	0.5	96	150.9	92	50
11 (2048 bins)	85dB	75	0.5	108	314.4	104	102.7

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	50	0.1	84	12.98	81	4.8
7 (128 bins)	85dB	50	0.1	103	28.37	99	10.4
8 (256 bins)	85dB	50	0.1	122	59.1	117	20.8
9 (512 bins)	85dB	50	0.1	142	124.5	136	42.3
10 (1024 bins)	85dB	50	0.1	162	255.2	156	84.7
11 (2048 bins)	85dB	50	0.1	183	533.1	176	174.3

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	50	0.5	74	12.0	71	4.17
7 (128 bins)	85dB	50	0.5	91	25.9	87	9.0
8 (256 bins)	85dB	50	0.5	108	53.3	103	18.0
9 (512 bins)	85dB	50	0.5	125	111.0	120	36.8
10 (1024 bins)	85dB	50	0.5	143	226.4	137	74.3
11 (2048 bins)	85dB	50	0.5	162	471.6	155	153.4

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	75	0.1	60	9.6	57	4.1
7 (128 bins)	95dB	75	0.1	73	20.6	70	7.6
8 (256 bins)	95dB	75	0.1	86	42.3	83	14.5
9 (512 bins)	95dB	75	0.1	100	88.4	96	29.8
10 (1024 bins)	95dB	75	0.1	115	180.7	110	59.7
11 (2048 bins)	95dB	75	0.1	130	376.9	125	122.9

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	75	0.5	55	8.6	53	4.1
7 (128 bins)	95dB	75	0.5	67	18.7	64	7.6
8 (256 bins)	95dB	75	0.5	79	38.9	76	14.5
9 (512 bins)	95dB	75	0.5	92	81.2	89	28.4
10 (1024 bins)	95dB	75	0.5	105	165.8	101	56.2
11 (2048 bins)	95dB	75	0.5	119	345.6	114	114.5

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	50	0.1	93	15.8	89	6.2
7 (128 bins)	95dB	50	0.1	114	33.1	109	11.8
8 (256 bins)	95dB	50	0.1	135	67.7	130	22.9
9 (512 bins)	95dB	50	0.1	157	140.8	151	46.5
10 (1024 bins)	95dB	50	0.1	180	287.0	173	93.7
11 (2048 bins)	95dB	50	0.1	204	597.6	196	193.7

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	50	0.5	84	12.98	81	4.8
7 (128 bins)	95dB	50	0.5	103	28.37	99	10.4
8 (256 bins)	95dB	50	0.5	122	59.1	117	20.8
9 (512 bins)	95dB	50	0.5	142	124.5	136	42.3
10 (1024 bins)	95dB	50	0.5	162	255.2	156	84.7
11 (2048 bins)	95dB	50	0.5	183	533.1	176	174.3

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	75	0.1	65	8.6	62	4.1
7 (128 bins)	105dB	75	0.1	80	20.6	76	8.3
8 (256 bins)	105dB	75	0.1	94	44.2	90	15.9
9 (512 bins)	105dB	75	0.1	110	94.2	104	32.6
10 (1024 bins)	105dB	75	0.1	125	194.2	119	65.2
11 (2048 bins)	105dB	75	0.1	141	406.7	135	134.0

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	75	0.5	60	9.6	57	4.1
7 (128 bins)	105dB	75	0.5	73	20.6	70	7.6
8 (256 bins)	105dB	75	0.5	86	42.3	83	14.5
9 (512 bins)	105dB	75	0.5	100	88.4	96	29.8
10 (1024 bins)	105dB	75	0.5	115	180.7	110	59.7
11 (2048 bins)	105dB	75	0.5	130	376.9	125	122.9

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	50	0.1	98	17.3	94	6.2
7 (128 bins)	105dB	50	0.1	120	35.5	115	12.5
8 (256 bins)	105dB	50	0.1	142	71.6	136	24.3
9 (512 bins)	105dB	50	0.1	166	148.5	159	49.3
10 (1024 bins)	105dB	50	0.1	189	302.4	182	99.3
11 (2048 bins)	105dB	50	0.1	214	629.3	206	204.8

	PFT input of 12 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	50	0.5	89	13.4	85	4.8
7 (128 bins)	105dB	50	0.5	109	29.8	105	10.4
8 (256 bins)	105dB	50	0.5	129	62.5	124	20.8
9 (512 bins)	105dB	50	0.5	150	131.7	144	43.0
10 (1024 bins)	105dB	50	0.5	171	270.1	165	87.5
11 (2048 bins)	105dB	50	0.5	194	564.4	186	181.9

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	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	75	0.1	63	9.6	60	4.1
7 (128 bins)	85dB	75	0.1	77	21.15	74	8.3
8 (256 bins)	85dB	75	0.1	90	43.7	87	15.9
9 (512 bins)	85dB	75	0.1	105	91.3	101	31.2
10 (1024 bins)	85dB	75	0.1	120	186.5	115	61.8
11 (2048 bins)	85dB	75	0.1	135	387.5	130	126.3

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	75	0.5	57	8.6	55	4.1
7 (128 bins)	85dB	75	0.5	70	19.2	67	7.6
8 (256 bins)	85dB	75	0.5	82	39.9	79	14.5
9 (512 bins)	85dB	75	0.5	96	83.1	92	28.4
10 (1024 bins)	85dB	75	0.5	109	169.7	105	56.2
11 (2048 bins)	85dB	75	0.5	123	352.4	118	115.2

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	50	0.1	97	15.38	93	5.5
7 (128 bins)	85dB	50	0.1	118	33.17	113	11.8
8 (256 bins)	85dB	50	0.1	139	68.2	134	23.6
9 (512 bins)	85dB	50	0.1	162	141.8	156	47.2
10 (1024 bins)	85dB	50	0.1	185	288.9	177	94.4
11 (2048 bins)	85dB	50	0.1	208	599.5	200	194.4

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	85dB	50	0.5	85	12.9	82	4.8
7 (128 bins)	85dB	50	0.5	104	28.3	100	10.2
8 (256 bins)	85dB	50	0.5	123	59.1	118	20.8
9 (512 bins)	85dB	50	0.5	143	124.0	137	41.6
10 (1024 bins)	85dB	50	0.5	163	253.8	157	83.3
11 (2048 bins)	85dB	50	0.5	184	527.8	177	171.5

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	75	0.1	64	10.1	66	4.1
7 (128 bins)	95dB	75	0.1	84	22.6	80	8.3
8 (256 bins)	95dB	75	0.1	99	47.1	95	16.6
9 (512 bins)	95dB	75	0.1	115	99.0	110	33.3
10 (1024 bins)	95dB	75	0.1	131	202.8	125	66.6
11 (2048 bins)	95dB	75	0.1	147	422.1	142	137.5

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	75	0.5	63	9.6	60	4.1
7 (128 bins)	95dB	75	0.5	77	21.15	74	8.3
8 (256 bins)	95dB	75	0.5	90	43.7	87	15.9
9 (512 bins)	95dB	75	0.5	105	91.3	101	31.2
10 (1024 bins)	95dB	75	0.5	120	186.5	115	61.8
11 (2048 bins)	95dB	75	0.5	135	387.5	130	126.3

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	50	0.1	109	16.3	105	6.2
7 (128 bins)	95dB	50	0.1	133	36.0	127	12.5
8 (256 bins)	95dB	50	0.1	157	75.0	150	25.0
9 (512 bins)	95dB	50	0.1	182	157.2	175	51.3
10 (1024 bins)	95dB	50	0.1	207	321.6	199	104.1
11 (2048 bins)	95dB	50	0.1	234	668.7	225	215.9

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	95dB	50	0.5	97	15.38	93	5.5
7 (128 bins)	95dB	50	0.5	118	33.17	113	11.8
8 (256 bins)	95dB	50	0.5	139	68.2	134	23.6
9 (512 bins)	95dB	50	0.5	162	141.8	156	47.2
10 (1024 bins)	95dB	50	0.5	185	288.9	177	94.4
11 (2048 bins)	95dB	50	0.5	208	599.5	200	194.4

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	75	0.1	74	11.5	71	4.1
7 (128 bins)	105dB	75	0.1	90	25.0	87	9.0
8 (256 bins)	105dB	75	0.1	107	51.9	103	18.0
9 (512 bins)	105dB	75	0.1	124	108.1	119	36.1
10 (1024 bins)	105dB	75	0.1	141	220.6	136	72.2
11 (2048 bins)	105dB	75	0.1	160	458.1	153	148.6

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	75	0.5	68	10.1	66	4.1
7 (128 bins)	105dB	75	0.5	84	22.6	80	8.3
8 (256 bins)	105dB	75	0.5	99	47.1	95	16.6
9 (512 bins)	105dB	75	0.5	115	99.0	110	33.3
10 (1024 bins)	105dB	75	0.5	131	202.8	125	66.6
11 (2048 bins)	105dB	75	0.5	147	422.1	142	137.5

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	50	0.1	112	19.2	108	8.3
7 (128 bins)	105dB	50	0.1	138	39.9	132	15.2
8 (256 bins)	105dB	50	0.1	163	80.7	156	28.4
9 (512 bins)	105dB	50	0.1	189	167.3	182	56.2
10 (1024 bins)	105dB	50	0.1	216	340.3	207	111.8
11 (2048 bins)	105dB	50	0.1	244	705.7	234	229.1

	PFT input of 14 bits at up to 128 Msps complex			Xilinx VirtexXCV3200E		Xilinx VirtexXC2V6000	
Stages	**Stop Band Atten**	**Overlap (%)**	**Cumulative Ripple**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**	**CLBs (% of FPGA)**	**Block RAMs (% of FPGA)**
6 (64 bins)	105dB	50	0.5	103	15.3	99	4.8
7 (128 bins)	105dB	50	0.5	126	34.1	121	11.1
8 (256 bins)	105dB	50	0.5	148	71.15	143	22.9
9 (512 bins)	105dB	50	0.5	172	149.0	166	47.9
10 (1024 bins)	105dB	50	0.5	196	304.8	189	97.9
11 (2048 bins)	105dB	50	0.5	222	633.6	213	203.4

Specifications Subject to change without notice.