Fully-Integrated 10 GHz CMOS VCO for multi-band WLAN applications

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Abstract

A 10 Ghz VCO, with 26% tuning range and with -96 dBc/Hz phase noise @ 100kHz offset, has been fabricated in a standard low cost 0.18um CMOS technology with a thick metal option.

In order to optimize this VCO for integration in a dual-mode 2.4/5 GHz transceiver product, a 6 bits-trimmable LC-tank with Q ranging from 12 to 18 has been first fabricated and characterized. The use of an on-chip transformer allowed measurements of the VCO to be made in different biasing conditions. This VCO can be used adequately to fit frequency synthezisers requirements for the 802.11a/b/g standards.

Introduction

Direct conversion radios for the 802.11a/b/g standards requires the development of synthesizers being able to reach the 2.4 GHz band, the 4.9 GHz band for japanese applications, the 5.15 Ghz and 5.35 GHz bands, and the 5.85 GHz band for european applications. Therefore the goal of our work was to develop a single 10 GHz VCO whose effective range is 9.6 GHz to 11.7 Ghz (21.8% tuning range). The design of the VCO required high-Q inductors and high-Q varactors to be customly engineered and modelled. The VCO core was intended to be used at the input of a frequency division chain. Therefore we designed first a 10 GHz frequency divider and output buffers at around 5 GHz. This divider has been characterized separetely in order to be able to extract real measurements of the VCO core.

High-Q tank and passive elements

As no passive elements were qualified on the technology for use at 10 GHz, high-Q center-tapped inductors with values ranging from 200pH to 1nH, as well as differential MOS varactors were seperately fabricated. The ASITIC software [1] was used to target inductors values within 5% (average) of measurements. All passive elements were characterized with on-wafer S-parameters measurements up to 40 GHz with a network analyser (Agilent 8722). Five differents shields (active and polysilicon shields) have been tested on the 200pH inductor to improve the quality factor. Measurements of the Q factor of both the inductors and the MOS varactors were expected to be noisy due to the relatively low values (<400 mOhms) of the series resistors involved. Therefore indivual sites were only used to get relative Q factors between elements. Absolute values were extracted from on chip resonnance where the combination of an inductor and a MOS varactor gives the possibility to measure Rp, the parallel resonnance impedance, with much higher precision. Fig1. shows measurements from this tank at different values of the varactor biasing.

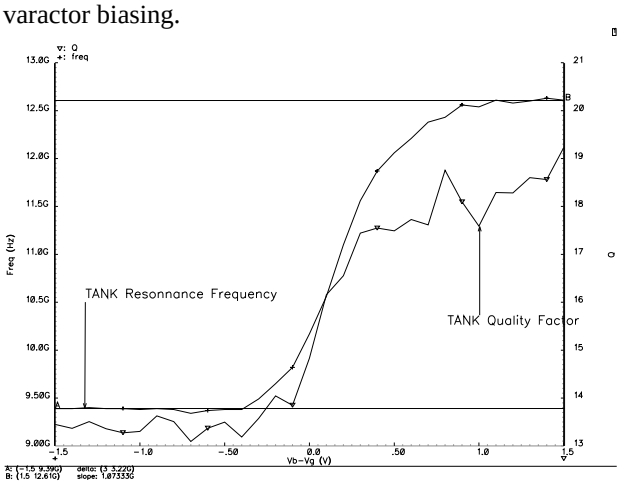

Fig 1. Resonnance Frequency and Quality Factor of an integrated Tank vs the Control voltage of the varactors.

Within the tank, the 240pH inductor has a quality factor of 22 @10 GHz. ASITIC was calculting 230pH and a Q of 22 @10 GHz. This 240pH inductor was drawn as single turn thick metal wire and has also been coupled with a second turn drawn with the same geometry on the metal layer just below to form a transformer. This transformer, characterized separetely, had a measured coupling factor of 0.9.

The MOS varactor used was an N-MOS in an N-WELL (accumulation mode varactor). 0.18um x 1.5um fingers were used to reduce both the gate resistance and the channel resistance. We chose here to give away tuning range for quality factor by using so small geometries. The fingers were combined into a fully differential structure to create a unit-cell with differential RF ports (the alternating gates) and a body biasing control voltage (common NWELL voltage). 65 of this unit cells were used in parallel to create an array of 6 bits (2^6-1) with 2 elements used for analog control. Fig1. is showing measurements when the 6 bits and the 2 'analog' elements are merged into the same control voltage. Q of the varactor is ranging from 33 @9.6 GHz (in accumulation) to 51 @ 12.6 Ghz (in depletion). The raw tuning range of this tank from -1.5V to 1.5V is about 31%.

We used for the modeling of the varactor a custom model in veriloga derived from a simplified BSIM3 charge model [2]. Fit accuracy is shown in Fig 2. in the case of small-signal.

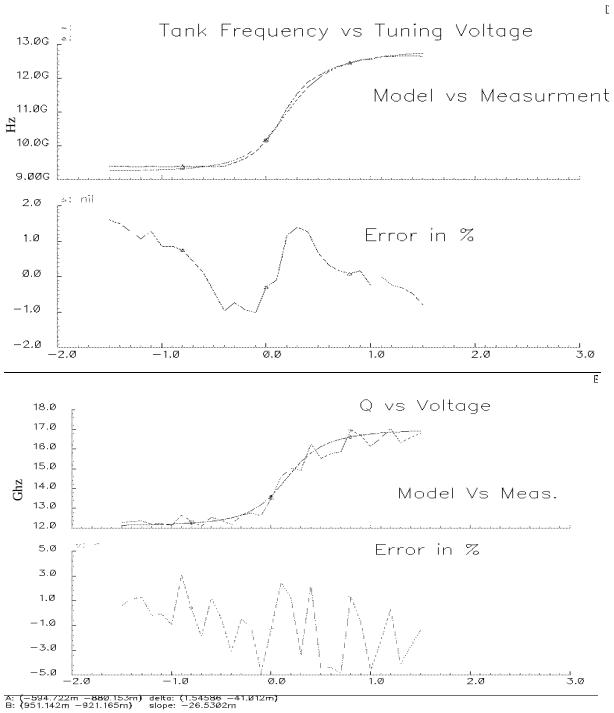

Fig 2. Tank model vs Measurement: Fit Accuracy

VCO core design

The design of the VCO core has been largely constrained by the achievable tuning range. Using larger inductor values would have forced the so-called unit-cell in the varactor array to be inferior to 10fF. Tuning range would have then been reduced by any parasitic capacitance. For the resonnance tank, we used the tank measured previously, replacing the inductor by the transformer. The use of PMOS was not possible because of the too strong impact of the Cgs on the tuning range compared to the gain in Gm. The schematic of the VCO core is presented in Fig 3. and is based on the Armstrong oscillator topology. Gates of the varactor array are DC biased by the middle point of the primary turn, ie *VDDVCO*. Therefore the control voltages of the array are relative to *VDDVCO* in this topology.

In this design, the biasing of all nodes of the differential crossed coupled NMOS pairs are accessible though chip pads. For the same *VDDVCO*, we are able to find, during the measurement, the optimum bias point of the crossed coupled-pair in order to reach an optimum between power consumption, phase-noise and output-power. *VDDVCO* can be set from 700mV to 1.8V. Current consumption can be adjusted by the DC bias of the gates of the crossed-coupled pair.

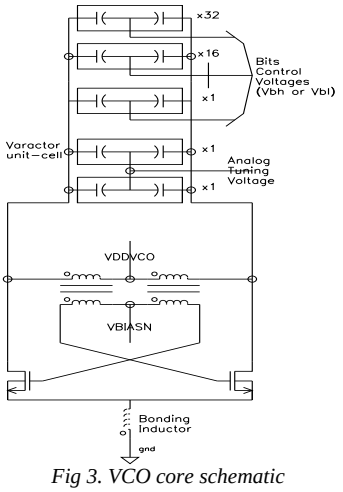

Fig 3. VCO core schematic

In the varactor array, 6 groups of varactor unit-cells are used as bits, ie in full depletion or in full accumulation, where the capacitance varies slowly with the control voltages. The residual frequency gain on the higher control voltage (*Vbh* in depletion) used for the bits is called *KVCO_bh* and the one used for the lower control voltage (*Vbl* in accumulation) is called *KVCO_bl*. These residual frequency sensitivities are not negligible since they were, in simulation, of the same magnitude than the frequency sensitivity from the 'analog' control voltage of the VCO (*KVCO*). In order to minimize the noise and spurious injection from the bits control voltages, it was important to reach full depletion and full accumulation. In order to have *KVCO_bh=KVCO_bl= KVCO*, at least 2.5V of control voltage range was needed (see Fig 2.). However at 10 GHz no AC coupling on the varactor elements, that would allow to double the control voltage range, was permitted. In order to create a voltage higher than *VDDVCO* control voltage, we designed a charge pump clocked at 40 MHz that creates *Vbh* and *Vbl*. *Vbh* was equal to *VDDVCO+VREF* and *Vbl=VDDVCO-VREF*, where *VREF* is a low noise reference voltage. The second advantage to this solution is the referencing of the control voltage to *VDDVCO*. Therefore if *VREF* has a good power supply rejection, the differential control voltages across the varactor elements are independent of *VDDVCO* (*VDDVCO+VREF-VDDVCO*). Two charge pumps have been used in parallel, one clocked on the rising edge of the 40 MHz clock and one on the falling edge. Therefore by matching, most of the created spurious power would be at 80 MHz. The schematic of the charge pump sub-circuit creating *Vbh=VDDVCO+VREF* is shown in Fig 4. Higher than VDD voltage can be created without the use of thick oxide because, with the use of the tripple well option, bulks of NMOS's can be raised to a intermediate potential to reduce the risk of punch-thru. The varactor elements face a maximum of *VREF* in DC and *VREF* plus the VCO amplitude at 10GHz. The *Vbh* and *Vbl* multiplexers towards the varactor arrays were realized by digitally control 'analog registers'. This charge pump does not have to provide any DC power besides the NWELLs and multiplexers leakage.

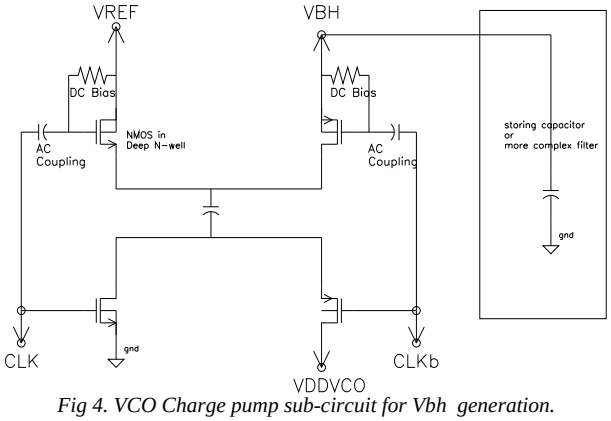

Fig 4. VCO Charge pump sub-circuit for Vbh generation.

The output of the VCO was taken on the primary turn of the transformer feeding directly the frequency divider.

Frequency divider and buffers

The schematic of the frequency divider is shown in Fig 5. It is based on a CML topology where current sources have been removed for head-room purposes. It provides in-phase and quadrature signals at 5 GHz. The core is loaded symetrically by two differential buffers that performs differential to single-ended transformation using on-chip transformers. The signal are then connected to the pad.

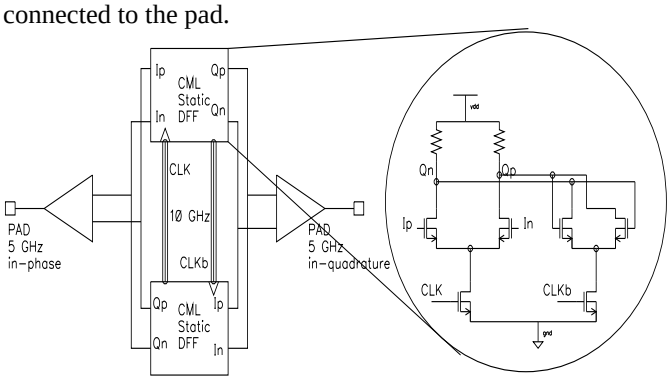

Fig 5. Divider topology

A standalone divider was fabricated on the same chip in order to make sure that the close-to-the-carrier noise of the divider were negligible compared to the VCO core expectation. A limitation on the maximum input frequency , measured at 9 GHz (spec. = 12 GHz) was found after the tape-out release. The reason was found in post layout simulations showing a buffer size too large limiting the speed of the divider core . The future versions of the divider implements larger core size and smaller buffer size to reduce this phenemenon .

Phase noise of the divider (Fig 6.) was better than the reference source at 8.5 GHz from 10 Hz to 1 Mhz frequency offset from the carrier. At 1 Mhz offset, the noise floor (-150 dBc/Hz) of the divider is reached.

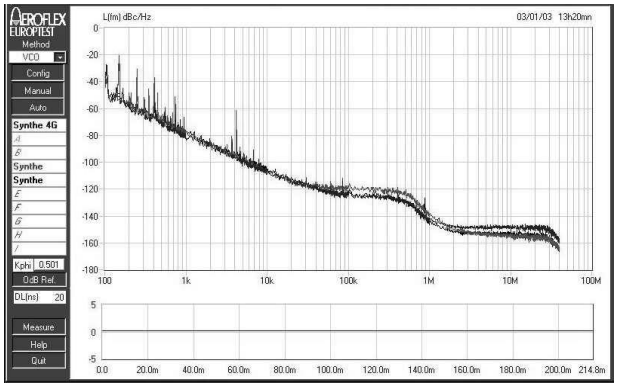

Fig 6. Phase noise measurement of the divider and of the RF 8.5 Ghz reference source.

Measurements

An Europtest PN9000 has been used to analyse the phase noise of the VCO (and the frequency divider). The method used is the delay line method. As the VCO charge pump was designed so that we could force *Vbh* and *Vbl* , and as the VCO is functional with *Vbh* of around 2.0V, the VCO has been mostly analyzed in a first step without its charge pump. The minimum *VDDVCO* useable for the measurements where set by the minimum input biasing voltage to have the divider functional. The maximum frequency, at which phase noise was measureable, was also set by the maximum functional frequency of the divider. This is the reason why we do not present phase noise at higher frequency. Results at 8.5 GHz are encouraging because the VCO tank has a lower Q at lower frequency and we expect better phase noise at higher frequency.

Phase noise

The VCO phase noise has been measured over different *Vbh*, *Vbl*, *VDDVCO*, *VBIASN* conditions. In Fig 7. VDDCO was 1.3V, *Vbh* was 2V, *Vbl* was 0V and *VBIASN* was 800mV. Power consumption was 11mA of the 1.3V power supply (14mW). The phase noise at 100kHz offest from a carrier at 4.28 GHz was -102dBc/Hz (Fig 7.) which leads to -96dBc/Hz at 8.56 Ghz knowing that the divider noise at 100 kHz offset is negligible. This correspond to a Figure of Merit (FOM [3][4]) of -183 dBc/Hz.

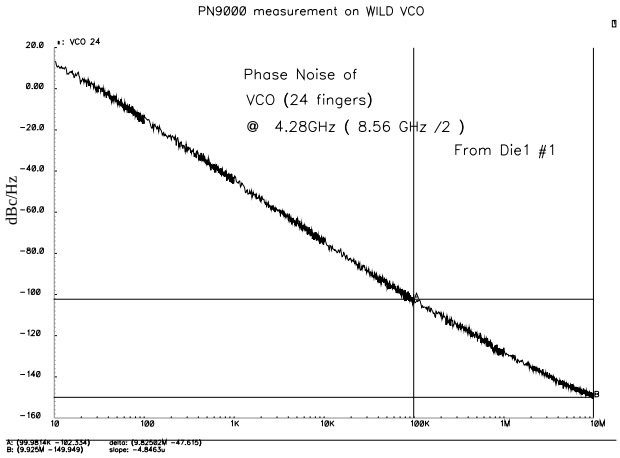

Fig 7. Phase Noise of the VCO at 8.5 GHz

Power consumption has been varied from 9mA to 14 mA (*VBIASN* from 700mV to 900mV) as well as control bits in the range allowed by the locking of the frequency divider . Phase noise at 100 kHz offset did not vary by more than 2dB.

Phase noise at 10 Mhz offset is -149dBc/Hz and is limited by the noise floor of the frequency divider.

Tuning Range

Tuning range is measured without the charge pump and with the frequency divider turned off because of the frequency divider limitation in frequency. We measure the peak at the VCO frequency of the leakage of the VCO through the frequency divider and its buffers. *Vbh (=Vp)* is set to 2V and *Vbl* to 0V. Fig 8. shows the 'analog' tuning curves at the maximum and the minimum trim settings on the varactor array. Fmax=10.73 GHz is taken on the upper curve at 1.4V on the 'analog' voltage, so that a PLL charge pump operating at 1.8V would have enough headroom. Fmin=8.51 GHz is taken on the lower curve at 0.4V for the same reason. This leads to a tuning range of 26.1%. This result is very encouraging knowing

that the effective tuning range is higher when *Vbh* is generated by the charge pump and therefore higher than 2V. This state of the art tuning range at 10 GHz has to be compared to the extremely low KVCO (< 100 MHz/V) on the 'analog' input. This makes the VCO a good candidate for an integration within a PLL because of its low frequency sensitivity to noise.

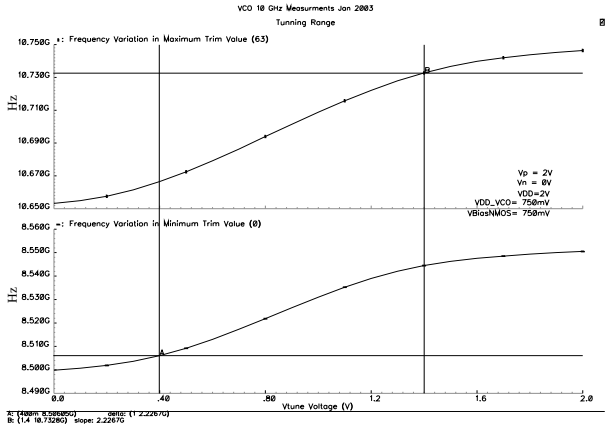

Fig 8. Tuning Range (without Charge Pump)

The center frequency will be shifted by 10% in the next version in order to be centered on the initial targeted center frequency.

Pushing issues

For the same reasons, we needed to measure the frequency sensitivity of the VCO to the *Vbh* and *Vbl* voltages. Measurements are shown if Fig 9.

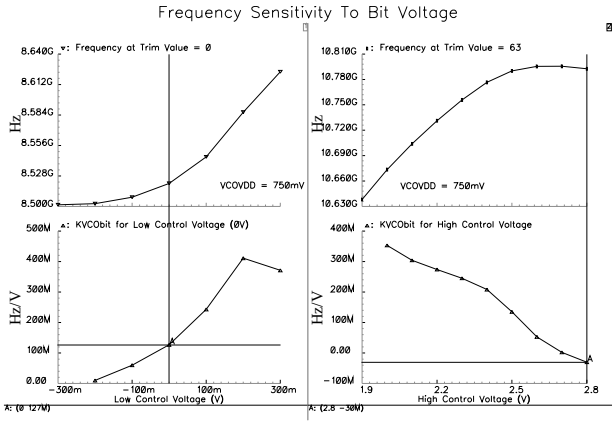

Fig 9. Frequency sensitivity to Vbh and Vbl

Frequency sensitivity to *VDDVCO* has been measured to be less than 100 Mhz/V (close in value to KVCO). In our PLL design, special biasing techniques on *VDDVCO* showed in simulation frequency sensitivity to power supply inferior to 10 Mhz/V.

VCO charge pump

Generated spurious were measured with a spectrum analyser after frequency division as well as with the frequency divider turned off. At 40 MHz offset, the spurious is 50dB down from the carrier. This can be increase of the VCO noise floor from -149dBc/Hz to -140dBc/Hz is been measured.

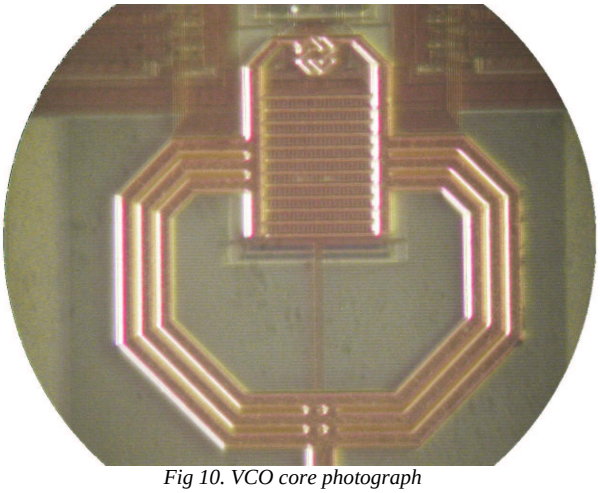

Fig 10. VCO core photograph

Conclusion

A state of the art VCO has been fabricated in a standard 0.18um CMOS process and measured. A 6-bits trimmable LC-tank that allows a tuning range of 26% at 9.6 GHz (2.2 GHz range) while having a maximum frequency sensitivity on its tuning voltage of only 100 Mhz/V. Phase noise at 100 kHz offset from carrier is as low as -96 dBc/Hz. Power consumption is 14mW from a 1.3V power supply leadingto a figure of merit of -182 dBc/Hz. An innovative charge pump is used to reach MOS capacitor regions where frequency sensitivity are lowered.

Therefore this VCO is an extremely good condidate for an integration in a multi-band WLAN synthesizer. Our system-level work has proved that our synthesizer, currently in design, will meet requirements for 802.11a/b/g standards.

[1] A. M. Niknejad,"Modeling of Passive Elements with ASITIC," *invited paper at RFIC 2002.*

[2] Maget, J., Kraus, R., Tiebout," A Physical Model of a CMOS Varactor with High Capacitance Tuning Range and its Application to Simulate a Voltage Controlled Oscillator," *International Semiconductor Device Research Symposium (ISDRS) 2001, Washington D.C., USA, Dezember 2001*

[3] H.Ainspan, J.-O. Plouchart,"A Comparison of MOS Varactors in Fully-Integrated CMOS LC VCO's at 5 and 7 Ghz", *European Solid-State Circuits Conference 2000 proceedings.*

[4] W. De Cock and M.Steyaert,"A CMOS 10GHz Voltage Controlled LC-Oscillator with integrated high-Q inductor", *European Solid-State Circuits Conference 2001 proceedings.*