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# Design of reconfigurable RF front-end for multi-standard receiver using switchable passive networks

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**Abstract** For successful implementation of a multi-standard receiver, a reconfigurable receiver architecture and a reconfigurable component design technique are essential. In this paper, an adaptable receiver architecture and a reconfigurable RF design technique using a switchable passive network are proposed. To verify the proposed design technique, the reconfigurable mixer and QVCO are designed using a flexible matching network and flexible LC tank, respectively. The measurement results of each component well prove the usefulness of the switchable passive network.

**Keywords** Multi-standard receiver · Receiver architecture · Switchable passive network · Mixer · Flexible matching network · QVCO · Flexible LC tank

## 1 Introduction

Recently, multi-standard transceivers have been extensively researched to meet the various demands of wireless communications that include smooth migration to future generation wireless standards, convergence of wireless services and intercontinental roaming [1]. However, the design of a multi-standard transceiver poses challenges because it should be comparable with a single standard transceiver in size, cost, and power consumption, while satisfying each standard's requirements. These requirements call for the minimization of component number and a large scale of integration.

With the scaling of technology, CMOS is a promising technology for low power and high integration level design. Additionally, CMOS design enables the integration of analog/RF transceivers with a digital modem, thus it is a good fit for SoC (System on a Chip). There have been some designs of multi-standard transceivers in CMOS technology [2, 3]. However, designing in CMOS does not confirm the success of the multi-standard transceiver; that is, a reconfigurable transceiver architecture and reconfigurable RF/analog components are also needed.

In this paper, a reconfigurable receiver architecture and a reconfigurable RF design technique using a switchable passive network are proposed. The architecture and dynamic range requirement for covering WCDMA, 802.11 a/b/g WLAN, and WiBro with a single receiver chain is analyzed. And, a multi-standard reconfigurable mixer and QVCO (Quadrature Voltage Controlled Oscillator) are designed with a switchable passive network, and verified by measurement.

The paper is organized as follows. Section 2 presents the proposed multi-standard receiver architecture, and Section 3 introduces a reconfigurable RF design technique using a switchable passive network. Sections 4 and 5 deal with the design and measurements of the multi-standard mixer and QVCO with switchable passive network; and Section 6 offers our conclusions.

## 2 Multi-standard receiver architecture

An ideal multi-standard receiver is a SDR (software defined radio), which is a single chip single path receiver whose

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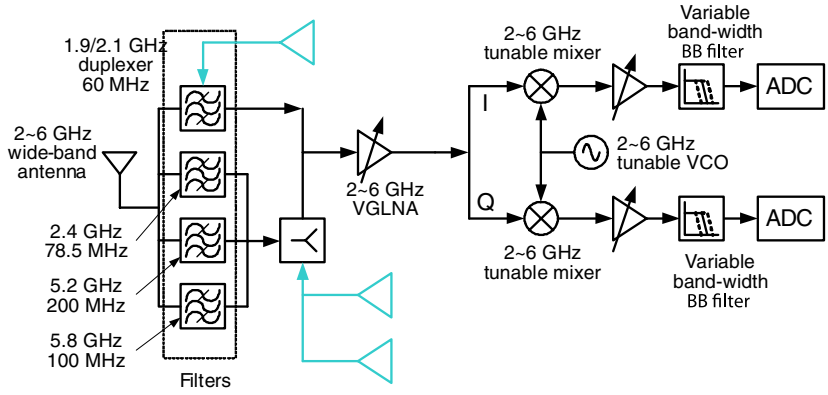


**Fig. 1** Proposed 2–6 GHz multi-standard receiver architecture

operation can be adapted to the environment by software program. However, thus far there has never been reported a receiver which covers multi-standards with a single path.

In traditional implementation of multi-standard receivers, multi-standard operation is achieved with independent RF front-ends supporting each standard [4]. However, it is undesirable because cost, size and weight increase as the number of target standards increases.

As stated before, a multi-standard receiver should be comparable with a single standard transceiver in size, cost, and power consumption; thus, the receiver architecture should enable reuse of components. Figure 1 shows the proposed multi-standard receiver architecture.

Target applications of this work are WCDMA, 802.11 a/b/g/n WLAN, and WiBro which are in the frequency range from 2 GHz to 6 GHz. The general characteristics of target standards are summarized in Table 1. In the proposed architecture, all the standards share the same RF/analog chain after LNA. However, there are several considerations for multi-standard such as architecture and dynamic range.

Direct conversion and low-IF are architectures of choice for high integration design. Due to low frequency error performance, direct conversion is good for standards with wide signal bandwidth, and low-IF is good for standards with narrow signal bandwidth. The high ADC (analog to digital converter) sampling speed requirement also limits the use of low IF architecture for standards with wide signal bandwidth (i.e. ADC for an 802.11a system with 10 MHz IF needs 40 Msps for Nyquist sampling and 80 Msps for four times over-sampling). As the WCDMA standard has relatively narrow bandwidth and tight sensitivity requirements, the 802.11 a/b/g WLAN and WiBro standards adopt a direct conversion architecture, and the WCDMA standard adopts a low-IF architecture as shown in Fig. 1. Figure 2(a), shows the base-band representation of down converted signals. The poly-phase processing, for image rejection in low-IF architecture, is done after analog to digital conversion, and this makes it possible to reuse a base-band filter for different architectures.

**Table 1** General characteristics of target standards

| | Duplexing | Frequency (GHz) | Channel spacing/BW (MHz) |
|---|---|---|---|
| WCDMA | FDD | 2.11–2.17 | 5/3.84 |
| 802.11b (g) | TDD | 2.405–2.4835 | 25/22 (20/20) |
| 802.11a | TDD | 5.15–5.35 | 20/20 |
| | | 5.725–5.825 | |
| WiBro | TDD | 2.3–2.4 | 10/10 |

The dynamic range requirement for a receiver is set by the sensitivity level, interference level, and maximum input signal level. However, in the multi-standard receiver the dynamic range requirement is even more stringent, because the power levels for sensitivity, interference and maximum signal vary according to standards. The most critical case is the sensitivity level in WCDMA (−107 dBm) and the maximum signal level in 802.11b WLAN (−10 dBm); thus the receiver should operate with 97 dB dynamic range. This dynamic range can be obtained by gain control of the LNA and base-band amplifier.

Another dynamic range issue is about ADC. The ADC dynamic range is in a trade-off relation with the base-band filter performance. If the base-band filter is just a low pass filter with 11 MHz cut-off frequency, then the interferers at 10 MHz offset from the WCDMA signal will reach ADC

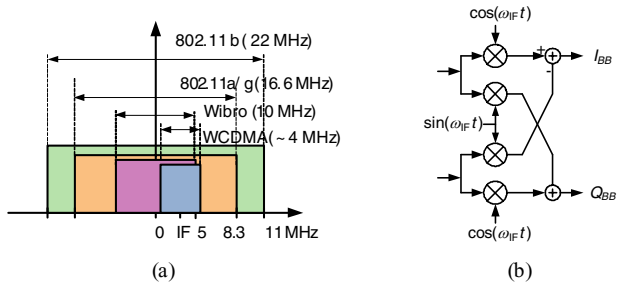


**Fig. 2** Signal processing in proposed receiver architecture: (a) Base-band representation of downconverted signal and (b) Poly-phase processing in digital domain

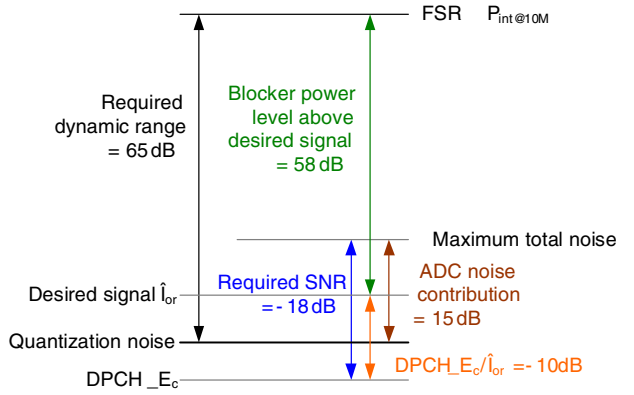


**Fig. 3** Diagram for the calculation of required dynamic range at ADC

without any filtering. In this case, the inter-modulation rejection test requires the dynamic range to be higher than 65 dB. Figure 3 shows a diagram of the calculation of required dynamic range at ADC. Here FSR is the full scale range of ADC, $\hat{I}_{or}$ is the power level of the received desired signal, and DPCH_$E_c/\hat{I}_{or}$ is the power level of the data signal. From Eq. (1), the required resolution of ADC can be calculated as 10 bit.

$$\mathrm{SNR}_{\mathrm{ADC}} = 6 \times N + 1.76 + 10 \log\left(\frac{f_{\mathrm{sample}}}{2 \times BW}\right) \geq 65 \quad (1)$$

This large dynamic range requirement of ADC can be mitigated by a variable bandwidth base-band filter, which is usually designed as a Gm-C filter [5].

The largest obstacles for single chip integration of the multi-standard receiver are RF band-selection filters, which are usually implemented as bulky SAW (surface acoustic wave) filters. One package implementation of SAW filters [6], MEMS switches and filters [7], and FBAR [8] are important research topics to minimize the size of RF filters. Variable center frequency/bandwidth LC filters [9] are also being researched.

## 3 Switchable passive network for reconfigurable design

LC resonator circuits are widely used in RFIC design. Used as a matching network or load impedance, the LC resonator circuit provides optimum performance in the frequency of interest. However, the narrow band characteristics of the LC resonator are obstacles for multi-band design. This shortcoming of the LC resonator circuit can be overcome by a few methods such as wide-band design, concurrent tuning, and center frequency tuning.

The wide-band design technique [10] is based on the wide-band filter design method. By controlling pole and zero of the network's transfer function, the center frequency and bandwidth can be controlled. The concurrent design technique [11] obtains desired circuit characteristics at multi-band simultaneously by adding resonant circuit(s) in series (parallel) with the input (output) matching network. However, these two methods are not reconfigurable, and a circuit designed by these methods may suffer from spurious responses.

Tuning of the resonant center frequency can be done in a few ways, i.e., by using the varactor, tunable active inductor [12], and switched capacitor array [13, 14] or switched inductor array [15]. But all conventional tuning methods have limitations. The tuning range that can be achieved by a varactor is limited to 10–20%; thus, it is not sufficient for the multi-standard receiver. Tuning with an active inductor may achieve very wide tuning range, but it's noisy and power consuming. The switched capacitor array or switched inductor array alone suffer from large power consumption at low frequency or discontinuous tuning.

In this paper, a switchable passive network is proposed as a multi-standard design technique. By combinational use of the switched capacitor array and switched inductor array, the switchable passive network maximizes the flexibility of front-end circuit design. In the following subsections, the operational principle and usage of the switchable passive network will be described.

### 3.1 Switchable passive network as an input matching network

Figure 4 shows a flexible input matching network using a switchable passive network. The flexible input-matching network consists of a switchable inductor array with $N$ series inductors and switches, and a switchable capacitor array with $M$ parallel capacitor and switches. The flexible input matching network can control a component's input impedance by adaptive control of switches according to operation frequency.

Through transistor analyses work, the input impedance of the mixer looking into the input matching network can be modeled as a series $R_{\mathrm{in}}$-$L_{\mathrm{in}}$-$C_{\mathrm{in}}$ network, as shown in Fig. 5 [16].

$$Z_{\mathrm{in}} = R_{\mathrm{in}} + j\omega L_{\mathrm{in}} + \frac{1}{j\omega C_{\mathrm{in}}}, \quad (2)$$

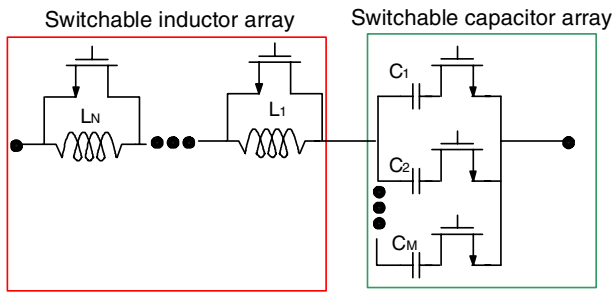


**Fig. 4** Flexible input matching network

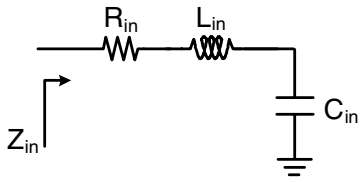


**Fig. 5** Simple input impedance model of matching network including input transistor

where $R_{\text{in}}$, $L_{\text{in}}$, and $C_{\text{in}}$ are

$$R_{\text{in}} \approx R_A \left( \frac{C_A}{C_P + C_A} \right)^2 \tag{3}$$

$$L_{\text{in}} \approx L_{\text{sw}} \tag{4}$$

$$C_{\text{in}} = C_p + C_A, \tag{5}$$

$R_A$ and $C_A$ are

$$R_A = R_{\text{on}} + R_{\text{tr}} \tag{6}$$

$$C_A = \frac{C_{\text{sw}} C_{\text{tr}}}{C_{\text{sw}} + C_{\text{tr}}}, \tag{7}$$

and $R_{\text{tr}}$ and $C_{\text{tr}}$ are

$$R_{\text{tr}} = R_g + \frac{R_o(C_{\text{gd}} + C_o)}{C_{gd}(1 + gm\, R_o)} \left( \frac{C_{\text{gd}}(1 + gm\, R_o)}{C_{\text{gs}} + C_{\text{gd}}(1 + gm\, R_o)} \right)^2 \tag{8}$$

$$C_{\text{tr}} = C_{\text{gs}} + (1 + gm\, R_o) C_{\text{gd}}. \tag{9}$$

To simplify the derivation of input impedance, the switching transistor is modeled as turn-on-resistance, $R_{\text{on}}$, and parasitic capacitance, $C_p$, as functions of the control voltage. $C_{\text{sw}}$ and $L_{\text{sw}}$ are capacitance and inductance value from switchable passive network, respectively, whose values are determined as combinations of capacitances and inductances from the capacitor and inductor array. As shown in this figure, input reactance is a function of $L_{\text{sw}}$, $C_{\text{sw}}$, $C_{\text{tr}}$ and $C_p$. For the special case of input impedance matching, $R_{\text{in}}$ can be adjusted to nearly certain impedance (i.e. 50 Ω) by appropriate selection of $C_p$, $R_{\text{on}}$ and $C_{\text{sw}}$.

### 3.2 Switchable passive network as an LC tank of VCO

The flexible LC tank for VCO consists of a switchable inductor array with N series inductors and switches, and a switchable capacitor array with M parallel capacitors, switches, and a varactor. Figure 6 shows the schematic of the flexible LC tank. By control of switches and the varactor, the resonant frequency of the LC tank can be varied, and the oscillation frequency of the oscillator can be varied accordingly.

**Table 2** Equations for the maximum and minimum values of tank reactance

| | | |
|---|---|---|
| Reactance from switchable capacitor array | $C_{\text{sc-max}}$ | $C_1 + C_2 + \cdots + C_M$ |
| | $C_{\text{sc-min}}$ | $\left(\frac{1}{C_1} + \frac{1}{C_{d1}}\right)^{-1} + \cdots + \left(\frac{1}{C_M} + \frac{1}{C_{dM}}\right)^{-1}$ |
| Reactance from switchable inductor array | $L_{\text{sl\_max}}$ | $L_1 + L_2 + \cdots + L_N$ |
| | $L_{\text{sl\_min}}$ | $L_1$ |
| | $C_{\text{sl\_max}}$ | $C_{\text{par},L1} + C_{\text{par},L2} + \cdots + \frac{1}{2} C_{\text{par},LN}$ |
| | $C_{\text{sl\_min}}$ | $\frac{1}{2} C_{\text{par},L1}$ |

*$C_{\text{dm}}$: $m$th switch transistor's drain capacitance, $C_{\text{par,Ln}}$: the parasitic capacitances from nth inductance.

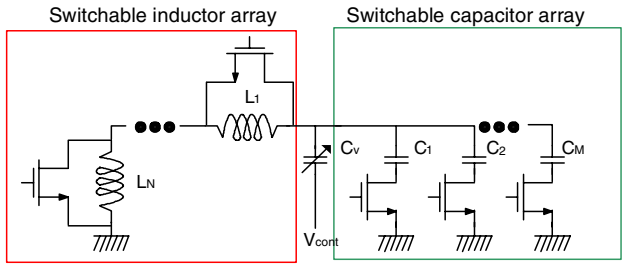


**Fig. 6** Flexible LC tank

Table 2 summarizes the maximum and minimum value of tank reactance from the switchable capacitor array and the switchable inductance array. By controlling the capacitance from the switchable capacitor array and the varactor and the inductance from the switchable inductor array to their minimum, the maximum oscillation frequency can be obtained. And, by controlling them to their maximum, the minimum oscillation frequency can be obtained.

## 4 Reconfigurable mixer with flexible input matching network

To verify the operation of the flexible input matching network, a PCB board is implemented with a mixer chip and off-chip flexible matching network [16]. Figures 7 and 8 show, respectively, a schematic diagram of the designed mixer schematic and a photo of the implemented PCB board. The off-chip flexible matching network consists of three inductors and three capacitors. The values of each inductor and capacitor are shown in Table 3.

Figure 9 shows the flexible matching network and its modes of operation. The operation of the network can be

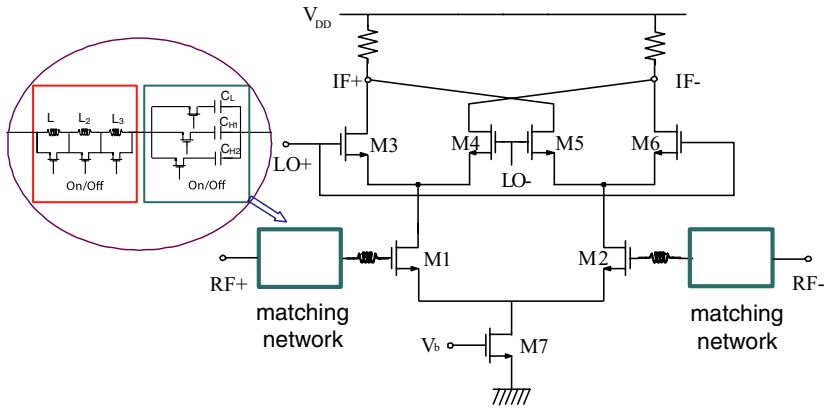


**Fig. 7** Reconfigurable mixer schematic

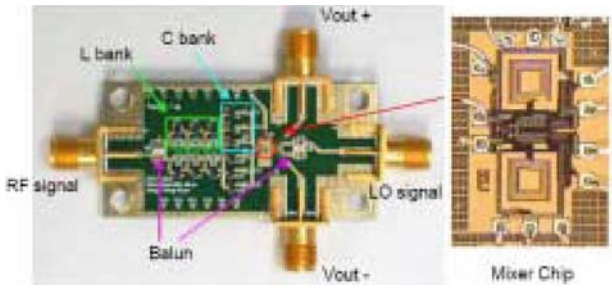


**Fig. 8** PCB board for the mixer test

divided into two modes: low frequency mode and high frequency mode. The low frequency mode covers from 2 GHz to 4.5 GHz. In this mode a fixed capacitance, $C_L$, with relatively high value, is active, and the reactance value is changed by switching series inductors in $L$ bank. On the other hand, at high frequency mode, 4.5–6 GHz, the reactance value is changed by switching capacitors in $C$ bank, while only $L_1$ in $L$ bank is kept active. $C_{H1}$ or $C_{H2}$ is selected and combined with $L_1$ for the choice of operation frequency.

As the matching network is off-chip, the switches are implemented with commercial BJTs. Some performance losses come from the non-ideality of the switches; in addition, the parasitic capacitances cause a frequency shift in matching condition and the parasitic resistances cause NF degradation. However, the effect of parasitic capacitance can be estimated by simulation during the design process, and NF degradation may be kept less than 1 dB using switches with large width.

**Table 3** The values of implemented inductors and capacitors

| | | |
|---|---|---|
| Inductance values of $L$ bank | $L_1$ | 2 nH |
| | $L_2$ | 3 nH |
| | $L_3$ | 4.3 nH |
| Capacitance values of $C$ bank | $C_L$ | 47 pF |
| | $C_{H1}$ | 0.5 pF |
| | $C_{H2}$ | 1.2 pF |

Figure 10 shows the $S_{11}$ response of the mixer with switch control. The measured return loss is somewhat worse than the simulation result. However, it follows a similar variation tendency to that of the simulation result; therefore, the operation of the matching network can be verified. In Table 4, the mixer's performances in three frequency bands are summarized. The conversion voltage gain is 3–5 dB lower than the simulation value, and the NF is roughly similar to the simulation results. The measured input $P_{1dB}$ and IIP3 values are a little bit higher than those of the simulation. The differences between simulation and measurement results mainly come from the loss in the external input matching network which is caused by parasitics in the implementation such as the stub parasitic, soldering parasitic and so on. Errors in measurement may contribute to the differences as well.

## 5 Reconfigurable LC QVCO with flexible LC tank

The reconfigurable LC QVCO is designed in 0.18 $\mu$m CMOS technology [17]. Figures 11 and 12 show a full schematic and chip photo of the designed VCO, respectively. The VCO is of complementary topology, i.e., MN1–MN4 and MP1–MP4 are switching transistors that compensate for the loss in LC tanks. To minimize the contribution of coupling transistors to phase noise, the VCO adopted SIPC (Source Injection Parallel Coupled) QVCO architecture [18]. MN5–MN8 lock the two differential VCOs in quadrature phase relation by the injection of $2\omega_0$ signal to the common source nodes. Additionally, by substituting the current sources with inductors, the phase noise performance of the VCO is further enhanced by eliminating the phase noise contribution from current sources.

The LC tanks of the QVCO are designed using a switchable passive network and are composed of three inductors (two of them are center-tapped), six capacitors (three for each output node), and two varactors for each differential oscillator. The half circuit of designed flexible LC tank is shown in

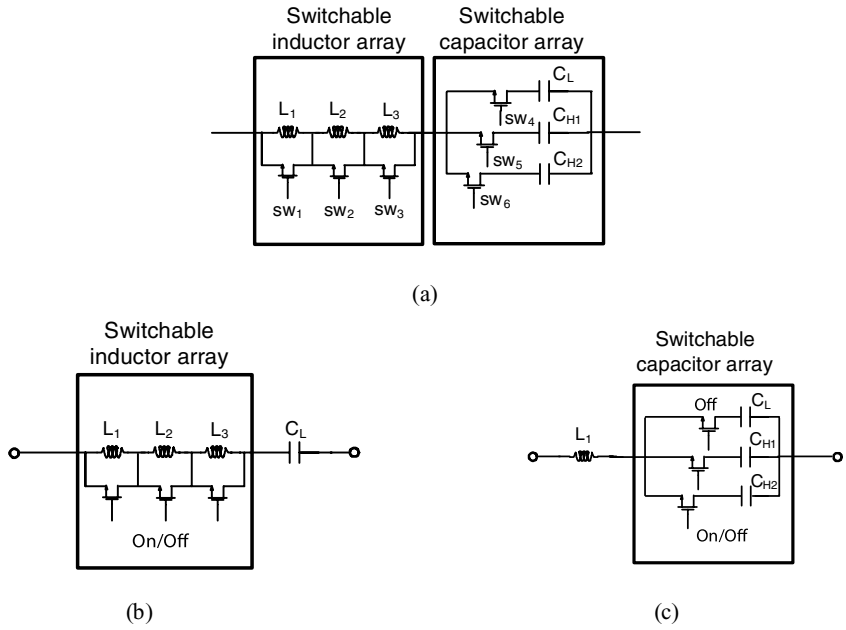


**Fig. 9** Proposed flexible matching network and operation: (a) Proposed flexible network, (b) Low frequency mode operation, and (c) High frequency mode operation

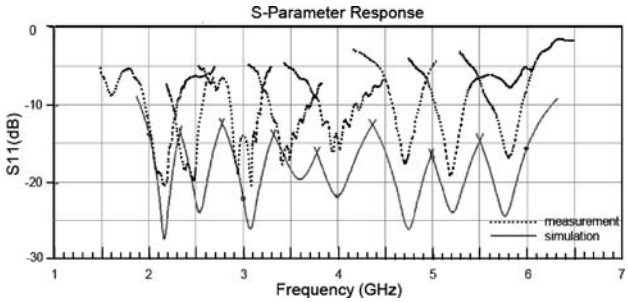


**Fig. 10** Return loss measurement

Fig. 13. The value of $L_1$ is 1.25 nH, $L_2$ is 2.3 nH, and $C_a$ is 135 fF. To minimize $Q$ factor degradation, inductor switches are of large enough width at 320 um/0.18 um. The sizes of the capacitor switches are binary weighted as the capacitors in the capacitor bank at 20 um/0.18 um, 40 um/0.18 um and 80 um/0.18 um, respectively. The minimum possible length is used for each switch to minimize the parasitics.

The supply voltage and current consumption are 1.5 V and 10 mA, respectively. The frequency tuning characteristics of the VCO are shown in Fig. 14. With the control of the switches, very wide tuning is achieved in two separate frequency bands, 1.73 ~ 2.49 GHz (37%) and 4.13–4.89 GHz (17%). When the inductor switches are on, only the smallest capacitance is used to tune the VCO due to relatively small inductance. However, if supply voltage and DC current are increased to 1.8 V and 12 mA, the tuning range at high band can be increased to 3.12–4.89 GHz (44%). The measured phase noise is −112 dBc/Hz@1 MHz in low band and −101 dBc/Hz@1 MHz in high band. Table 5 summarizes the measured performances and compares them with the simulation results.

The measured tuning ranges are shifted about 15%, and phase noise performances are worse than simulated performance by 10 dB in both bands of operation. This performance degradation is mainly due to the parasitics from the long inter-connection line between spiral inductors. After considering the parasitics from the inter-connection line by momentum simulation, the discrepancies between measured tuning ranges and simulated ones are about 5%.

**Table 4** Mixer performance summary

| Performance | 2.1 GHz (WCDMA) | | 2.4 GHz (IEEE 802.11b,g) | | 5.2 GHz (IEEE 802.11a) | |
|---|---|---|---|---|---|---|
| | Sim. | Meas. | Sim. | Meas. | Sim. | Meas. |
| Conversion gain (dB) | 14.1 | 9.5 | 13.4 | 8.3 | 9.2 | 6.2 |
| NF (dB) | 13 | 13.8 | 10.5 | 12.1 | 14.3 | 14.8 |
| Input P1dB (dBm) | −14.9 | −12.7 | −14.5 | −11.7 | −12.7 | −10.2 |
| IIP3 (dBm) | −3.9 | −2.1 | −3.8 | −1.9 | −2.1 | −1.1 |
| S11 (dB) | <20 | <19 | <20 | <17.6 | <25 | <13.9 |
| Current (mA) | 4.85 | 6 | 4.85 | 6 | 4.85 | 6 |
| Supply voltage (V) | 2.5 | | | | | |

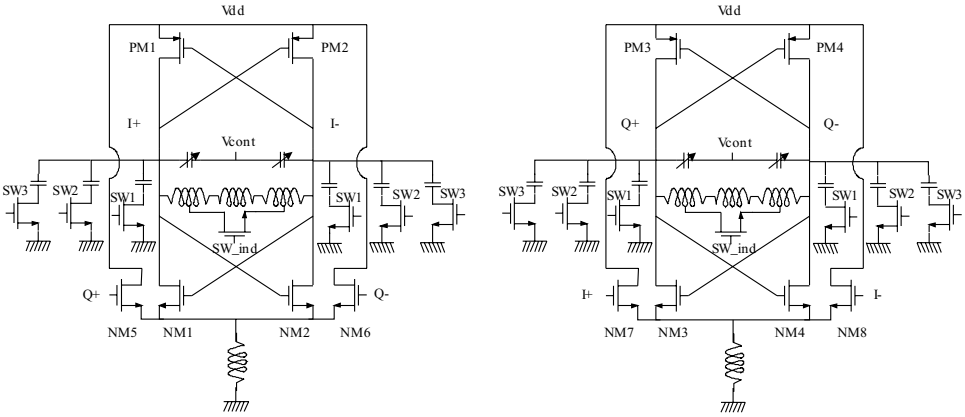


**Fig. 11** Full schematic of the designed VCO

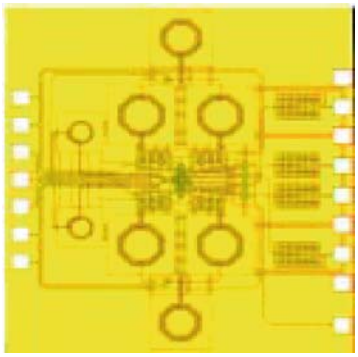

**Fig. 12** Chip photo of the designed VCO

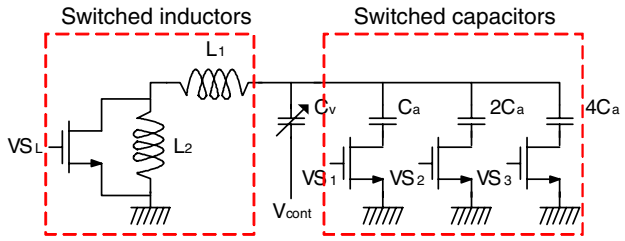


**Fig. 13** Schematic of the flexible LC tank (Half)

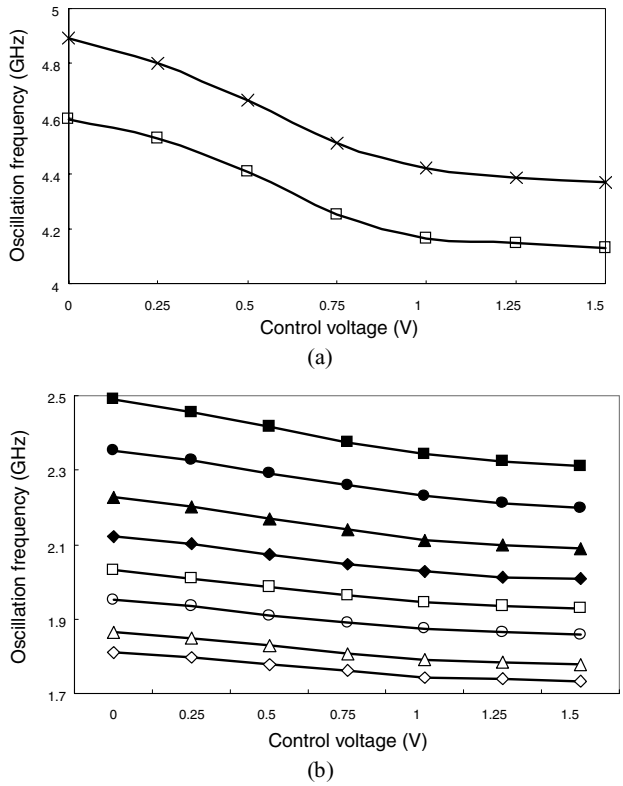


**Fig. 14** Frequency tuning characteristics of the VCO: (a) High operation frequency and (b) low operation frequency

## 6 Conclusion

In this paper, an adaptable receiver architecture and a reconfigurable RF design technique using a switchable passive network are proposed and analyzed. The reconfigurable mixer and VCO are designed using a switchable passive network as a matching network and LC tank, respectively. The measured results are very close to the simulation results. Therefore, we can conclude that the proposed design technique is useful for multi-band component design.

**Table 5** Summary of measurement result and comparison with simulation result

| | | Low band | High band |
|---|---|---|---|
| Tuning range (GHz) | Sim. | 1.94–3 | 4.9–6 |
| | Meas. | 1.73–2.49 | 4.13–4.89 |
| Phase noise (dBc/Hz@1 MHz) | Sim. | − 122 | − 114 |
| | Meas. | − 112 | − 101 |
| DC current (mA@1.5 V) | Sim. | 10 | |
| | Meas. | 10 | |

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