ENABLING TECHNOLOGIES FOR SOFTWARE DEFINED RADIO[1]

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ABSTRACT

The choice of building blocks and communications infrastructure are the most critical part of any Software Define Radio (SDR) for both commercial and military applications. They both share similar challenges towards implementation of a true SDR. A true SDR is facing numerous hardware and software challenges, many of them are still to be addressed by undergoing research. There are several publications and references concerning software architecture and requirements of a SDR, and the technology requirements are tend to be sidelined. This is mainly because of the fact that in the JTRS program, the focus is on voice and low data rate applications; also the frequency band is limited to UHF. On the other hand, the cost of the implementation is less of a concern for now. However, by emerging of advance warfare technology where it is required to transport more bits per warrior to accommodate video and telemetry data, and also by introducing initiatives similar to the JTRS to other communication systems, such as satellite and high-capacity tactical links, technology requirements of SDR have to be revisited.

In this paper the focus is on the hardware technology aspect of the SDR. The main technical objective of a SDR is a versatile reconfigurable platform, which provides interoperability. The main blocks of a true SDR are namely: intelligent antenna, programmable RF modules, high-performance Digital-to-Analog (DAC) and Analog-to-Digital Converters (ADC), Digital Signal Processing (DSP) techniques/technology and the interconnect technology.

I. INTRODUCTION

A SDR can be considered as an open architecture, which creates a communication platform by connecting modularized and standardized flexible hardware building blocks. Software load defines tasks and interconnections between the blocks and gives an identity to the system. SDR Forum describes SDRs as "radios that provide software control of a variety of modulation techniques, wide and narrow band operation, communication security functions, and waveform requirements of current and evolving standards over a broad frequency range" [1]. SDR concept promises the main solution for supporting a multitude of wireless communication services in a single infrastructure design.

As depicted in Fig. 1, any SDR architecture comprises of five main hardware elements: antenna, RF, analog/digital conversion, digital signal processing blocks and the interconnect backbone. Each block has to provide a considerable amount of flexibility while maintaining performance. In the following sections of the paper, the current state of the technology and the trend for each of the five mentioned block is briefly reviewed and discussed.

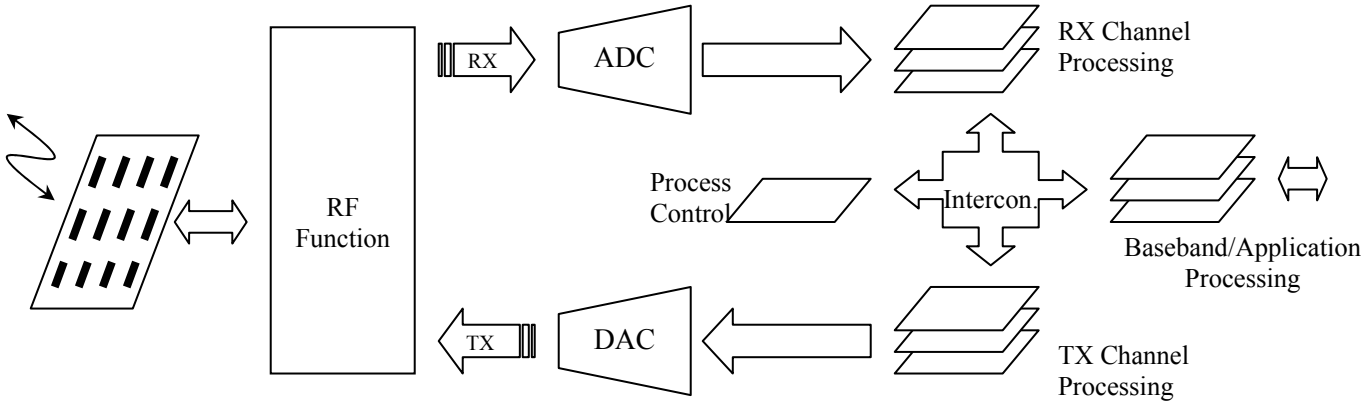


Figure 1 – Five elements of a SDR system

[1] This work was supported by Harris *SDR Center of Excellence*.

II. INTELLIGENT ANTENNA TECHNOLOGY

Antenna front-end can be split to the basic antenna element and the related array configuration and processing blocks. Today's antenna solutions for SDR systems are based on several separate antennas to cover a broad range of frequency. This is because, the traditional antenna design techniques limits the extent of application and performance of an antenna. In other words, since the antenna size is always proportional to the operating wavelength, a wideband antenna will be less performing and less cost effective than a narrowband antenna. Thus the main activities in this domain remain mainly in array processing blocks and techniques to make the antenna system more performing and intelligent. Array processing and beamforming techniques are fairly mature fields and wherever the cost of implementation has not been the driving factor, they have been deployed.

The word intelligent covers the very basic feature of frequency band selection and adaptation up to advance capabilities such as interference cancellation and mobile tracking. An ideal antenna for a SDR is a self-adapt, self-align and self-healing antenna, which is capable of complete adaptation to its required application and the transmission environment. Self-adaptability is a capability that the antenna system would adjust its basic parameters such as gain according to the selected frequency band and required system gain of the application. As soon as the system was set up, self-alignment enables the antenna to direct itself based on the maximum signal reception with an aid provided by a telemetry data or a Global Positioning System (GPS). Self-healing can be defined as a feature that helps the system to combat any friendly or hostile interference by proper use of techniques such as array processing, beam-steering and even variable-polarization.

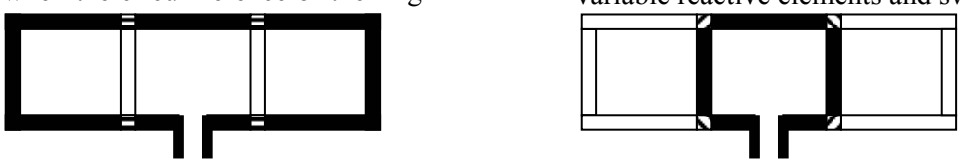
In order to fulfill the above-mentioned features, besides the required elegant signal processing techniques, high performance and flexible radiating elements are essential. Micro Electro-Mechanical System (MEMS) raises the hope for major breakthroughs in the field of broadband reconfigurable antenna design. For example, by employing MEMS, it is possible to change the operating frequency of a rectangular ring slot antenna electronically. In a square slot antenna, a good performance at a frequency is obtained, when the circumference of the ring is approximately one wavelength. By using MEMS switches, as shown in Figure 2, in order to reconfigure the antenna for a new frequency band, it is only required to switch in or out different slot elements. Therefore, a frequency change of 3 to 8GHz has been made possible [2, 3]. The main advantages of MEMS switch over PIN diode switch are low loss, high isolation and smaller size. They are all significant factors for an antenna system.

With a similar thought of switching in and out different elements of an antenna system, one may wish to have more granularity of radiating elements with a vast number of switches to allow virtually, any form of antenna realization. This could be the step beyond the MEMS technology for the antenna design that might use smart materials. The smart materials concept is a cross-disciplinary field that has attracted the attention for various applications [4]. Smart materials science promises, introducing materials with incorporated switches and sensors, a variation of them with proper electromagnetic behavior could constitute the main requirements to design and build configurable antennas. Based on this view, according to the selected performance requirements, the microelements of the antenna system will be routed to provide the required radiation pattern.

III. PROGRAMMABLE RF MODULES

One of the employed techniques for existing SDR systems is to use a bank of RF modules to cover the entire frequency band. By maturing the wideband synthesizer technology, low-noise high-performance semiconductor processes, very flexible RF modules are rising. Thanks to low loss and compactness of MEMS technology, implementation of high performance RF devices with a high level of integration of circuits including switches have been made possible. The moveable feature of MEMS devices allows dynamic adjustment of the component values. MEMS technology improves the performance and flexibility of several RF components such as [5, 6]:

- Low phase noise Voltage Controlled Oscillators (VCO) by using MEMS-based high Q resonators
- Wideband varactors and phase shifters by using MEMS-based variable capacitors and switch-capacitor networks
- Tunable filters by employing MEMS-based variable reactive elements and switches.



(a) (b)

Figure 2 – Application of MEMS switch for reconfigurable antenna, (a) $f_{opt}=f_a$, (b) $f_{opt}=2f_a$

The challenge for designing programmable bandpass filters remains to be resolved. They are essential in both transmitters and receivers, insuring efficient use of channel and high sensitivity. Bandpass filters are usually the most expensive items on the list for RF modules and at the same time the least flexible. A SDR implementation requires these elements to be either electronically configurable or to be stacked to forming a filter bank. Today most of SDR implementations rely on the latter. High *Q* MEMS-based filters have been demonstrated [5, 6].

Also, superconductive technology has enabled to implement tunable bandpass filters with ultra-sharp roll-off characteristics. A tune filter with a center frequency of 3.5GHz and a tuning range of 620MHz has been implemented by benefiting from superconducting thin film process [7]. The low loss nature of this process enables design and realization of multistage thin film filter with low insertion loss and broadband operation.

IV. DIGITAL-TO-ANALOG / ANALOG -TO- DIGITAL CONVERSION

SDR systems hinge on ADCs and DACs components. They have the unique tasks of conversion between analog to digital domain and vice versa. The flexibility of a SDR can be augmented significantly by pushing the converters closer to the antenna. Traditional electronic converters are pushing the envelope to achieve more resolution and faster conversion rates. However the demand for even higher performance is fueling novel techniques of conversion employing super-conductive and optical sampling techniques.

To the best knowledge of the author, the forerunner ADC implementation technology based on the traditional semiconductor approach is reported to achieve 6 bits resolution at 3.2GS/s and 10 bits resolution at 1GS/s. The used semiconductor technology is based on GaAs supporting an f_T=80GHz [8]. Also, the most performing DAC to date has a capability 12 bits resolution at a sampling rate of 1.3GHz. Since the receiver has always more complexity than the transmitter, the importance of operating at higher rates of conversions for ADCs is more significant and thus has attracted more effort than DACs.

At sampling rates ranging from 2Ms/s to 4Gs/s, resolution degrades by 1 bit for every doubling of the sampling rate. An analysis of SNR shows that the 1-bit per octave slope is related to the sample-to-sample variation of the instant in time at which sampling occurs. This variation is called aperture jitter or aperture uncertainty [9]. In an optically sampled ADC, the sampling and quantization functions are performed in the optical and the electronic domains, respectively [10 - 12]. The main advantage of an optically sampled ADC lies in low timing jitter of the mode-locked laser source. An SNR of 51dB equivalent to an effective resolution of 8.2 bits at a rate of 505MS/s is reported. A further improvement to achieve multi-GHz sampling with a 12 bits resolution is foreseen for near future [10, 11]. Also, generation of optical clock pulses with measured timing jitter as low as 16 *fs* (0.016%) and amplitude jitter of 0.058% for 3 *ps* wide pulses by a laser mode locked at 10 GHz is accomplished [8]. These jitter values will support a photonic sampling accuracy of 11 bits at 10 GS/s.

The other breakthrough technology that opens the door for increasing resolutions and speed of ADCs is Rapid Single Flux Quantum (RSFQ) [13 - 16]. This technology is based on a fundamental quantum mechanical property of superconductors, stating the existence of magnetic flux in discrete quantized form. In this technology single flux quantum pulses represent binary values. Since an integrated single flux quantum represent a pulse, the performance of the technology is strictly limited by the maximum slew-rate of the input signal. Hence, the performance of the technique is optimized by a trade-off between the resolution and the speed of processing. In an oversampled superconductive-based ADC, the effect of aperture jitter is reduced significantly; therefore very wideband operation becomes feasible. Superconductive ADCs operating at 19.6 GHz has been demonstrated [16]. One important note regarding these ADCs is that the sampling rate at the input is not the same as the output of the device. There is a programmable decimator inside the converter, which has to be set based on a trade-off between number of bits and the bandwidth. The other very important feature of a superconductive ADC is its high sensitivity. The minimum required power to drive SFQ circuit is less than 1 *u*W that is three order of magnitude less than 1 *m*W required power for a high speed semiconductor ADC. This feature coupled with high sampling rate eventually eliminates the necessity of a Low Noise Amplifier (LNA) and the resulting direct sampling at the antenna port leads to more system gain [7]. Although superconductive ADCs have not yet performed significantly better than semiconductor counterpart, the main essence of the technique is very promising.

Another front that is being explored for high speed ADC Implementation is based on "Σ−Δ" analog to digital conversion method [25-26]. The basic idea of Σ−Δ ADC is to trade sampling speed for number of bits. The Σ−Δ is consist of two parts. The first part is the Σ−Δ modulator and the second part is a low pass digital filter. The main benefits of a Σ−Δ based ADC are:

- Highpass filtering of the quantization noise which results higher signal to noise ration in the frequency range of interest
- Inherent linearity.

However, a Σ–Δ ADC depending the on the required resolution has to be oversampled by a several order of magnitude compared to the highest frequency of interest. Therefore due to the limitation of the sampling speed, Σ–Δ has not been yet considered for digital receiver applications. To address the problem, a high speed Σ–Δ ADC with a sampling rate of 18 GHz is reported in [27]. It yields a two tone SNR of 48dB, 42dB and 33dB for input signals at 150 MHz, 500 MHz and 990 MHz, respectively. The implemented ADC does not exhibit as great as expected in the performed simulations, however it indicates a new direction in ADC technology.

ADC Technology	Resolution	Speed	Status
Semiconductor Based	6 bits	3.2 GS/s	Commercially available April 2002
Optical Sampling	8.2 bits 12 bits	505 MS/s Multi GS/s	Experimental Proof of concept
Superconductor RSFQ	11 bits	175MS/s	Experimental
Σ–Δ	8 bits (150MHz)	18GS/s	Experimental

Table 1 – ADC technology comparison chart

Note: the resolution number and speed performance of superconductive and Σ–Δ ADCs are not fixed values and can be trade-off to achieve the desired performance.

V. DIGITAL SIGNAL PROCESSING TECHNIQUES

DSP is the principal enabling element of SDR. Embedded DSP algorithms in the processing engine are responsible to make all the promises of SDR come true. By employing an efficient DSP architecture and set of algorithms, proprietary waveforms and features can be implemented as the applications matures. Over the past 50 years, DSP has had significant contribution in evolution of communication systems. Compression, noise cancellation, multi-dimensional filtering, adaptive processing, detection, estimation and array processing are only a few areas that have had a major impact on several applications [17, 18]. Among several DSP techniques used in SDR platform, sampling techniques, rate conversion and multirate processing have been instrumental in progress and development of DSP-based systems [19].

Regular implementation choices are based on DSP-processors, ASICs, FPGAs as well as the emerging mixture of these technologies. There are continuous efforts, to increase the performance of all the three types of DSP engines. FPGAs are getting faster than ever and their internal building blocks are becoming more efficient. Inherited parallel processing capability of FPGAs and ASICs has made them the core-processing engine in many communication systems. Distributed DSP based on systolic arrays are evolving to compete with the performance of ASICs and FPGAs. Traditional DSP processors have achieved significant boost in speed by increasing the processing clock and also employing techniques such as Very Long Instruction Word (VLIW), however their performance still are not sufficient for many applications. In selection of a DSP engine, there are mainly five key selection criteria to be considered [20]:

- Programmability
- Level of integration
- Development cycle
- Performance
- Power.

In order to find the extension and envelope of each criteria, they have to be weighed against the cost target and the mission of the system.

VI. INTERCONNECT TECHNOLOGY

One of the main benefit or objective of the SDR is the ability to connect several independent building blocks to set-up a radio link. An open architecture system obliges a set of interface standards to be developed within framework of an interconnect technology. A successful interconnect approach has to address following critical issues [21]:

- Leveraging open standards
- Addressing multiple protocols
- Meeting increasing speed and throughput requirements
- Connecting to traditional circuit networks.

Mainly, there are three main interconnect architecture: bus architecture, switch fabric architecture and tree architecture [22].

In bus architecture, a bus connects different processing modules. Usually, a high-speed data bus provides high-speed data transmission between the functional units, and a lower speed bus is employed for low rate control data transactions. Based on this architecture, at any time, only one functional unit can transmit data on the bus. In other words, bus is time shared between the functional units. Bus assignment is done by a bus arbitration blocks, which processes requests and sets the priority. Time division limits the bandwidth and also restricts the scalability of the interconnect bus architecture. A new version of PCI, PCI-X allows the bus to run up to 133 MHz at 64 bits bus to accommodate a peak data rate of 1 Gbyte/s, however this seems to be still not enough for some applications. In general bus architectures such as VME and PCI benefit from easy implementation and widespread use in industry.

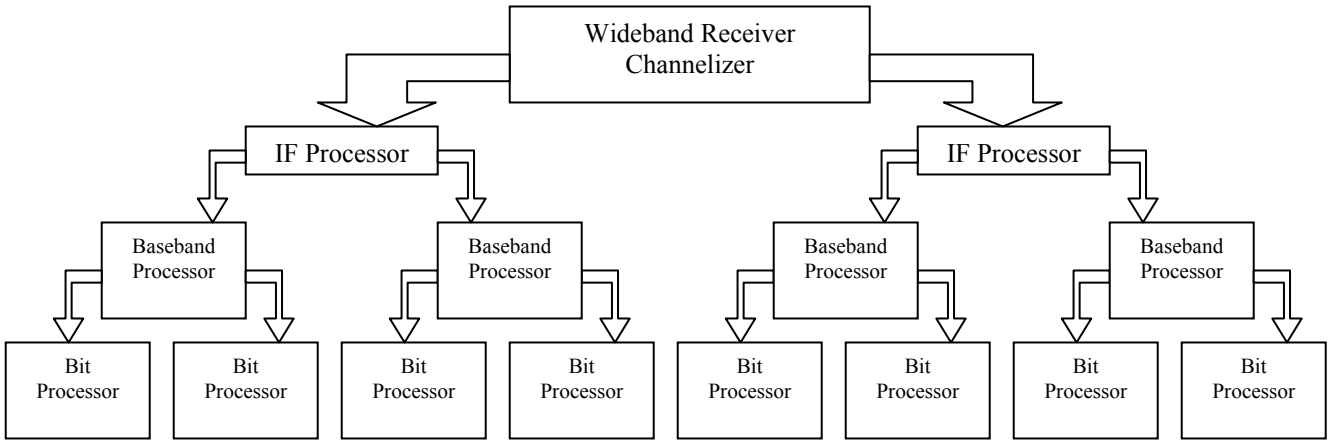


Figure 2 – Tree interconnect architecture

Bus architecture has some unique characteristics that make it difficult to be replaced entirely in near future.

In switch fabric architecture, there is an adapter in each functional unit that packages the data from the functional unit before being sent to the switch fabric. The principle of a switch fabric is similar to an IP or an ATM switch. Switch fabric technology has following advantages compared to the bus architecture [23]:

- High scalability in both slot count and aggregate performance
- Flexibility in physical configuration and size
- Cost-effective, high availability designs with no single points of system failure
- Efficiently addressing the disparate needs of different traffic types and communication protocols.

However it should be noted that the use of switch fabric architecture in SDR calls for strict requirement and performance on the switch fabric in terms of throughput and packet delay. Reference [24] provides a good summary of several interconnect technology based on the switch fabric.

As we may notice from Figure 1, in a wireless communication system the product term of *data rate* by *resolution bits* becomes lower and lower as we move from RF to IF and baseband processing. This suggests an architecture similar to a tree where from the root node to the leaf node, the channel width becomes wider and wider, Fig. 2. The tree architecture optimizes the use of interconnections and avoids providing interconnects between the blocks that do not require such provision. The main disadvantage of this architecture is its implementation and limited flexibility.

Table 2 summarizes basic features and drawbacks of each interconnect architecture. Basically, no single interconnect technology has yet been able to satisfy the broad range of applications and requirements. Thus the interconnect architecture for SDR systems will not be converged on any single solution in near future.

	Speed	**Complexity**	**Scalability**	**Applications**
Bus	Slow	Low	Low	Medium
Switch Fabric	Medium	Medium	High	High
Tree	Fast	High	Medium	Low

Table 2 – Interconnect architecture comparison chart

VII. CONCLUSION

In this paper, the five main technology elements of SDR are reviewed and the state of technology in each domain is explored. Also implementation approaches in each cased are compared. MEMS technology is becoming a critical enabling technology to extend the capability and performance of antennas and several RF building blocks. The resolution and sampling rate of signal converters are being continuously improved. The performance of ADCs is being enhanced by several distinguished effort of: advance semiconductor processes, superconductor based and optical sampling techniques. The final call in selection of a DSP implementation is based on: level of programmability and integration, development cycle, performance and power. Among the main three interconnect scheme, the bus interconnect enjoys the widespread use and recognition, however switch fabric with higher speed and more flexibility are being more prominent. In the paper some of the technical challenges of a SDR system are summarized and for each case enabling technologies were briefly discussed.

VIII. ACKNOWLEDGEMENT

The author would like to thank all the members of Harris SDR Center of Excellence for their support of this work.

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