Superconductor Analog-to-Digital Converters

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Invited Paper

Ultrafast switching speed, low power, natural quantization of magnetic flux, quantum accuracy, and low noise of cryogenic superconductor circuits enable fast and accurate data conversion between the analog and digital domains. Based on rapid single-flux quantum (RSFQ) logic, these integrated circuits are capable of achieving performance levels unattainable by any other technology. Two major classes of superconductor analog-to-digital converters (ADCs) are being developed—Nyquist sampling and oversampling converters. Complete systems with digital sampling at rates of ∼20 GHz and above have been demonstrated using low-temperature superconductor device technology. Some ADC components have also been implemented using high-temperature superconductors. Superconductor ADCs have unique applications in true digital-RF communications, broadband instrumentation, and digital sensor readout. Their designs, test results, and future development trends are reviewed.

Keywords*—Analog-to-digital converter (ADC), decimation filter, digital receiver, digitizer, flux quantum, rapid single-flux quantum (RSFQ), sigma delta modulator, signal-to-noise ratio (SNR), single-flux quantum (SFQ) pulse, software-defined radio, spur-free dynamic range (SFDR), superconducting quantum interference device (SQUID).*

I. INTRODUCTION

The relentless quest for higher performance of analog-to-digital converters (ADCs) is fundamental to progress in communications, radar, high-speed instrumentation, and sensor applications. For many applications, ADCs are the critical elements that define the architecture and the performance capabilities of the entire system. The present relatively slow progress in ADCs based on conventional silicon technology is not capable of matching the current rate of advancements in digital circuits available for increasingly sophisticated digital signal processing. A host of alternative technologies, ranging from III–V semiconductors to optics, are being pursued in order to develop ADCs with higher resolution and wider bandwidth.

Superconductor technology exhibits a set of characteristics uniquely suitable for the implementation of analog-to-digital conversion. It simultaneously includes high switching speed, low power, natural quantization, quantum accuracy, high sensitivity, and low noise [1]–[3]. Superconductor ADCs have already demonstrated superior performance in the laboratory [4], [5], and are now being developed into high-speed and precision instrumentation and communication systems.

This paper will survey the current state of the art of superconductor ADCs, starting with a background on superconductor ADCs. It will then continue in Section II with a survey of the various classes of superconductor ADCs, followed by a discussion in Section III of closely related circuits such as digital decimation filters. The paper will conclude with a description of some developing systems applications for these superconductor ADCs and expected trends in the near future.

A. Superconductor Technology for ADC

An ADC is an electronic circuit that converts an electrical signal from the analog domain (e.g., a continuous voltage or current) to the digital domain, typically providing N binary bits at a rate known as the sampling frequency f_s. Superconductor ADCs are capable of providing more bits at a higher f_s than any other technology and are at the threshold of commercialization. One can find earlier reviews and basics of superconductor ADCs in [6]–[8].

As described in the accompanying paper on superconducting digital electronics in this special issue [9], Josephson junctions exhibit switching speeds of the order of a few picoseconds or less, making them suitable for the highest speed digital circuits for computers and digital signal processors (DSPs). Another accompanying paper on superconducting quantum interference devices (SQUIDs) (a SQUID is an inductive loop with one or more Josephson junctions) [10]

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addresses the quantum-limited sensitivity and linearity of these devices for measuring magnetic fields and currents. Superconductor ADCs incorporate both SQUIDs and Josephson junction-based logic, taking advantage of their unique combination of speed, low power consumption, low noise, sensitivity, linearity, and dynamic range.

Superconductor ADCs are based on some of the special properties of superconductivity and Josephson junctions and circuits. Unlike conventional semiconductor circuits, the properties of superconductor circuits are closely related to the dynamics of magnetic flux Φ in these circuits [1]–[3]. In particular, the two fundamental principles of superconductor circuits are the following.

1) Conservation of flux in a superconducting loop.
2) Quantization of flux in a superconducting loop in integral multiples of the flux quantum, which is a fundamental value defined with Planck's constant h and electron charge e: $\Phi_0 = h/2e \cong 2.07 \times 10^{-15}$Wb $= 2.07$ mV $\cdot$ ps.

Together, these naturally occurring quantum phenomena set the current circulating around a closed superconducting loop with Josephson junctions to be fundamentally periodic in the analog magnetic flux applied to it. The threshold spacing of a superconductive loop is determined with the accuracy of fundamental constants. This *natural relationship* of analog and digital forms makes superconductor technology especially suitable for ADC implementation.

The current circulating around a closed superconducting loop with inductance will maintain a flux $n\Phi_0$ indefinitely, creating an ideal digital storage element. The function of a Josephson junction is to change the value of n. Physically, a Josephson junction is a weak link between two superconductors that consists of an ultrathin insulating layer; functionally, it acts as a controllable valve that permits flux quanta to leak out of (or be pumped into) a superconducting loop, one Φ_0 (or one fluxon) at a time. By Faraday's law $V = d\Phi/dt$, the corresponding voltage across the Josephson junction is a voltage pulse with integral $\int V dt = \Phi_0$. This is known as a single-flux quantum (SFQ) pulse. Such SFQ pulses are extremely narrow—typically $\sim$2 ps—and have a pulse height $\sim$1 mV. This is also an extremely low-power two-terminal switching element, with switching energy per pulse on the order of $I_c\Phi_0 \sim 2 \times 10^{-19}$ J or $\sim$1 eV. This makes the speed–power product (a typical figure of merit for comparison of different technologies) the ultimate leader among all other technologies.

The relationship between voltage and flux allows a Josephson junction to be used for *perfectly linear* data conversion. For example, if a dc voltage of 100 μV is applied across a Josephson junction, it will generate SFQ pulses at a rate of $V/\Phi_0 \cong 48$ GHz. Counting the pulse rate in a digital counter provides an ideal ADC. Alternatively, if one applies a combination of a dc current and an RF current at frequency f, then under appropriate conditions, the pulse generation by the junction will synchronize with the applied RF frequency, yielding a dc output voltage $V = \Phi_0 f$ (or integral multiples thereof). This provides the basis for an ideal digital-to-analog converter (DAC) [11], [12]. Practical Josephson data converters are more complicated than these simple examples but are based on similar concepts, as will be discussed later in this paper.

Superconductor ADCs and DACs, with extremely high sampling frequencies (tens to hundreds of gigahertz), require digital circuits capable of operating at similarly high data rates. The use of the same very narrow SFQ pulses forms the basis of rapid SFQ (RSFQ) logic, arguably the fastest digital technology [13]–[15], enabling integration of ultrafast RSFQ digital circuits with superconductor ADCs and DACs. Originally developed in mid-1980s [16]–[18], RSFQ logic now provides the foundation for virtually all of the fastest superconductor digital circuits being developed worldwide [9], [19]. Simple circuits have been demonstrated with speeds in excess of 750 GHz [20], and complex medium-scale integrated circuits (ICs) $\sim$30 GHz [19], [21], with performance up to 200 GHz projected in the not-too-distant future [22]. This is far faster than projected performance of competing technologies [23] and motivates much of the recent developments in the field of superconductor digital electronics.

B. ADC Background

There are two distinct aspects of the analog-to-digital conversion process: *sampling* and *quantization*, which deal with discretization in time and in magnitude, respectively. The quantization process introduces some error or "quantization noise" into the system. Of course, this is in addition to any noise present in the signal, as well as other noise sources, such as jitter in the sampling clock. Even if the quantization is precise, the clock frequency will limit the bandwidth of a signal in the digital domain. According to the Nyquist sampling theorem, a signal that is sampled at a frequency f_s can accurately represent an analog signal with bandwidth up to the Nyquist frequency $f_N = f_s/2$.

All superconductor ADCs generally fall into two categories: *Nyquist-sampling* ADCs and *oversampling* ADCs. An ideal Nyquist ADC samples a bandwidth-limited signal at a sampling rate $f_s = 2f_N$ and provides an accurate digital representation of that signal, with the only error associated with the quantization noise. Most commonly, this Nyquist ADC is composed of a large number of *separate quantizers*—single-bit comparators, each defining a single quantization level. In practice, the performance of such an ADC is limited by the precision of the quantization levels, which are often determined by resistor values in resistor networks.

In the alternative oversampling ADC approach, the signal is sampled at a frequency $f_s \gg 2f_N$ using a *single quantizer*. Then feedback techniques and digital filtering are used to decrease the quantization noise and enhance the effective dynamic range. Oversampling ADCs are built using a "delta" or more often a "delta–sigma" modulator (sometimes called "sigma–delta") [24]. Here delta (Δ) refers to difference and sigma (Σ) to sum, the discrete analogues of differentiation and integration.

Although both delta and delta–sigma modulators are very similar in implementation (Fig. 1), there are important differences between them. In the delta modulator [Fig. 1(a)], the difference (delta) between input signal and the feedback signal (the integrated output pulses) is digitized in the quantizer. The digital output represents the signal derivative, which should be integrated later in the following digital integrator to restore the input signal. The maximum range of this modulator is determined by signal slope (slew rate). In the delta ADC, the noise (after integrating) is essentially white, so that narrowing the output bandwidth will reduce the noise power proportionally to the bandwidth reduction.

In the delta–sigma modulator [Fig. 1(b)], the quantizer digitizes the sum (sigma) of differences (delta) of input signal and feedback signal (the sum of previous differences). Consequently, the digital output represents the input signal itself. The maximum modulator range is determined by signal amplitude. The quantization noise at the output is shaped, in that it is suppressed at low frequencies but enhanced at high frequencies approaching the Nyquist frequency. Decreasing the output bandwidth by filtering will increase the signal-to-noise ratio (SNR) inversely proportional to the third power, rather than simply linearly with bandwidth.

The overall ADC performances of both types of modulators are very similar, although the advantage of the delta ADCs grows for signals with the lower frequency components having the highest slew rate. Therefore, delta ADCs are preferable in applications when slew rate saturation is more manageable than amplitude saturation [24]. In semiconductor technology, more robust sigma–delta ADCs are overwhelmingly preferred to delta ADCs. This is partially due to the fact that bit errors (e.g., due to imperfect integrators) occurring from the delta modulator will accumulate and result in output offset. In superconductor technology, the availability of a close-to-ideal integrator in the feedback loop makes delta ADCs practical.

The state-of-the-art sigma–delta ADCs use higher order modulators with multiple feedback loops (typically four loops). This has the effect of further suppressing the quantization noise in the output spectrum. For example, a second-order modulator will exhibit a fourth power in noise as one moves up in frequency away from the signal. To date, only lower order ADC modulators have been implemented in superconductor technology.

Most superconductor ADCs demonstrated thus far are *low-pass* ADCs, which are designed to digitize any signal from dc up to some cutoff frequency of the input circuit. However, many RF applications consist of a narrow-band signal around a rather high RF frequency, and for these, a *band-pass* ADC would be more appropriate. In terms of sigma–delta ADCs, this requires suppressing the quantization noise around a higher frequency f_0, rather than at dc. This can be achieved by using a band-pass filter (such as a resonator) instead of an integrator in Fig. 1.

There are several standard characterizations for ADCs [25]. The SNR is the ratio of the signal power to the total noise power in the output bandwidth. A closely related quantity is the effective number of bits (ENOB), which is defined as $\text{ENOB} = (\text{SNR}_{\text{dB}} - 1.76)/6.02$. The ENOB is typically smaller than the number of hardware bits provided by the ADC and accounts for several possible sources of noise. The spur-free dynamic range (SFDR) represents the ratio of the signal amplitude to that of the highest spur (or spurious signal) within the relevant frequency band and is usually expressed in decibels (or sometimes in bits, by dividing by 6.02). The SFDR is normally larger than the SNR, since not all of the noise is concentrated in a single peak. The SFDR is a good measure of nonlinearity, since the highest spur is often at the second or third harmonic of the signal.

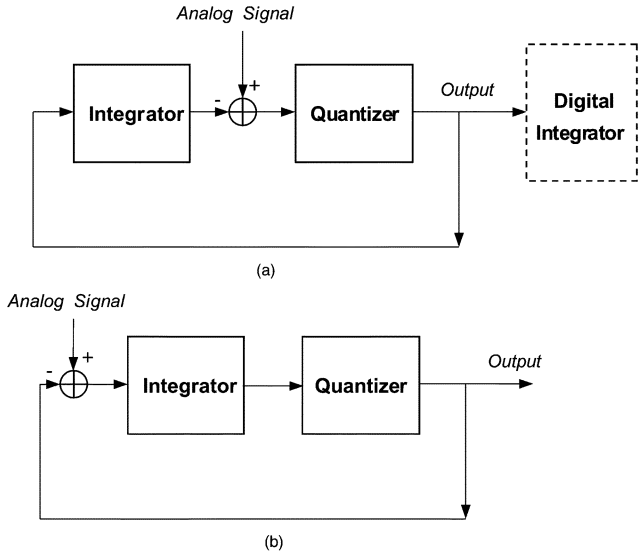


Fig. 1. Oversampling ADCs: discrete system diagrams for first-order: (a) delta and (b) delta–sigma ADC modulators.

There is a general tradeoff between the dynamic range of an ADC and the frequency bandwidth BW for any given device technology; the range decreases approximately in inverse proportion to the maximum frequency. This is partly because the device switching speed determines the maximum sampling frequency, which in turn limits the gain that may be obtained by oversampling a high-frequency signal. It is also due to the effect of timing jitter of the sampling clock which is proportional to the signal frequency. In addition, the larger bandwidth of higher frequency signals increases the total noise, thus reducing the ENOB. A summary plot of high-performance ADCs is shown in Fig. 2 (similar to that by Walden [25]), where the SNR and SFDR are plotted versus the output sample rate. The CMOS and SiGe–CMOS circuits are overwhelmingly preferred for commercial ADCs which dominate audio and low-megahertz frequency ranges and are also quite competitive in the gigahertz range. Fast III–V (GaAs or InP) circuits are also used to build special-purpose ADCs for high-megahertz and gigahertz ranges. For comparison, some recent data from superconductor ADCs are also shown (further details will be given later). Even in this early stage of development, using lithography with unsophisticated 3-μm Josephson junction sizes, the superconductor ADCs perform on a par with the best semiconductor ADCs. Further advances are anticipated as the lithographic scale and circuit yield are improved.

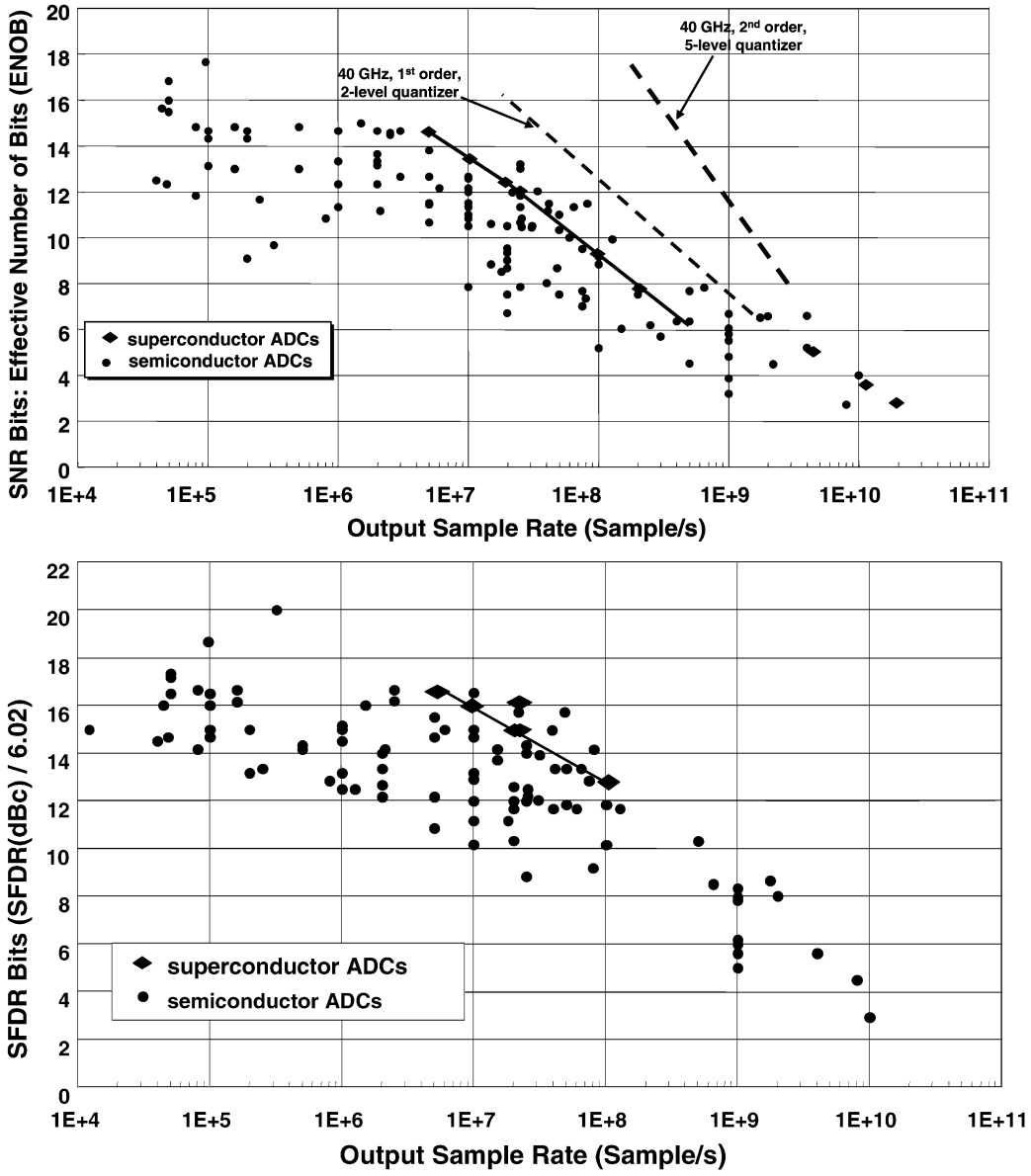


Fig. 2. Plot of SNR (top) and SFDR (bottom) versus sample rate (for signal at Nyquist frequency) for high-performance semiconductor (from [25] and recent ISSCC 2004 proceedings [http://www.isscc.org]) and superconductor ADCs (from [4], [5]). Dashed lines indicate the simulated superconductor ADC performance for quite modest 1.5-μm fabrication process.

There are three ways of increasing the dynamic range (SNR): 1) increasing the sampling rate (f_s); 2) increasing the number of quantization levels; and 3) increasing the order of the modulator. The SNR of an ideal oversampled delta–sigma modulator on the order of n, using an m-b quantizer, is given by

$$\text{SNR} = \frac{3}{2}\left(\frac{2n+1}{\pi^{2n}}\right)(2^m-1)^2 R^{2n+1} \qquad (1)$$

where $R = f_s/2\text{BW}$ is the oversampling ratio [24].

To increase sampling rate or clock speed, one must decrease device switching times and delays, which can be achieved by altering the device fabrication process, e.g., better lithography [22]. Increasing f_s from 20 to 40 GHz doubles the oversampling ratio, increasing SNR by $(6n+3)$ dB or $(n+0.5)$ b. For a first-order $(n=1)$ ADC, with $f_s = 40$ GHz and BW $= 10$ MHz, this gives 95 dB or just below 16 b. SNR may also be improved by increasing the number of quantization levels. If a 2-b quantizer is used instead of a 1-b quantizer, the dynamic range increases by 9.5 dB. However, the most dramatic improvement in SNR is obtained by increasing the order of the modulator. For a second-order $(n=2)$ 1-b quantizer ADC, with $f_s = 20$ GHz and BW $= 10$ MHz, the SNR is 139 dB or 23 b. However, for large oversampling ratio, it is often difficult to maintain the theoretical 2.5-b/octave (or 15-dB/octave) slope due to various circuit imperfections. Still, a real second-order modulator is expected to be far better than a first-order modulator.

C. Materials for Superconductor ADCs

Superconductor ADCs are medium-scale ICs requiring hundreds or thousands of Josephson junctions for complete systems. As such, they require a well controlled IC foundry, with reproducible junction properties. Most of the complete ADC circuits have been demonstrated thus far, primarily using low-temperature superconductor (LTS) niobium Josephson junctions, operating at about 4 K. As described in the accompanying review [26] on Josephson circuit fabrication, these Nb junctions are generally prepared using a standard thin-film multilayer process based on $Nb/AlO_x/Nb$ trilayer tunnel junctions, with critical current densities on the order of a few kiloamperes per square centimeter (kA/cm^2) for junction sizes of several micrometers. Since critically damped junctions are generally needed for these circuits (to avoid hysteretic *I-V* characteristics), they also require resistive shunts around the junctions, typically made using a metallic layer such as Mo or TiPd. The latter is not superconducting at millikelvin temperatures and is required for some sensor applications cooled to that temperature level. The circuits also require inductors, which are generally composed of Nb microstriplines, separated from a ground plane by an SiO_2 insulating layer. The standard process for making ADCs is practically identical to that for making RSFQ logic circuits and SQUIDs. These circuits are often operated immersed in a liquid helium bath, but can also function well when mounted on a closed-cycle refrigerator (or cryocooler) that maintains temperatures in the range 4–5 K. The total heat dissipation of such a circuit is very small, well below 10 mW, so that a properly designed cryopackage that minimizes external heat leaks can operate with less than 100 mW of total cooling power [27].

For some applications, superconductor ADCs operating at higher temperatures are also of interest despite some loss in performance due to higher noise properties. Josephson junction ICs based on niobium nitride (with T_c up to about 17 K) have also been demonstrated. NbN-based counting ADCs with 16-b resolution have been demonstrated to operate at 10 K for infrared (IR) sensor applications [28].

Operation at even higher temperature is possible using the high-temperature superconductors (HTS). There have been major efforts to develop a reproducible technology for Josephson junctions based on $YBa_2Cu_3O_7$ (YBCO), although the high temperatures required for epitaxial deposition of these materials makes a true multilayer process difficult to achieve. There has been some success in obtaining damped junctions with I_cR_n product on the order of 0.2 mV and with uniformities in critical current of better than 10% (1 sigma). For medium-scale ICs, one needs better uniformity and higher yield. To date, some key components of ADCs, including a simple first-order sigma–delta modulator, have been demonstrated [29]–[32]. Such an HTS circuit could operate at temperatures up to about 40 K and possibly higher, lessening the requirements on the cryogenic cooling system. However, it seems unlikely to have the HTS technology reach the required complexity in the near future. On the other hand, fast progress in compact cryocoolers has made Nb-based ADCs useful for a wider range of applications.

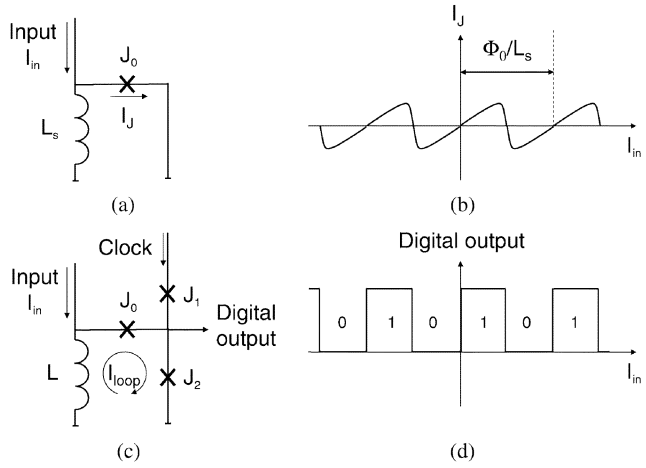


Fig. 3. (a) Schematic of a single junction SQUID acting as a flux quantizer. (b) Periodic SQUID transfer function. (c) Schematic of the comparator with clocked sampling circuit. (d) Comparator digital output.

One of the key features of Nb RSFQ ICs is that their characteristic clock speeds, already very high (tens of gigahertz), are expected to increase by up to another factor of 10 in the next decade as the junction scale is decreased to submicrometer dimensions, and the integration scale is increased accordingly [22]. This should yield substantial improvement in the speed-resolution tradeoff of superconductor ADCs.

II. Types of Superconductor ADCs

A. Superconductor Nyquist ADC: Flash ADC

In a conventional flash ADC, a set of comparators, clocked simultaneously, digitizes an analog input into an n-b digital word. In this type of ADC, both *quantization* and *sampling* occur at the same time. The primary advantage of this Nyquist-rate parallel ADC is the fast conversion speed. Therefore, it is ideal for digitization of wideband and transient waveforms. However, the number of required comparators is $2^n - 1$, one for each quantization level, which grows exponentially with the number of output bits n, making scaling to large number of bits difficult. It is possible to reduce somewhat the number of required comparators using more advanced Nyquist-rate ADC architectures.

In contrast, a superconductor flash ADC, based on SQUID comparators, provides a unique solution for drastic reduction of circuit complexity, and at the same time, allows faster sampling. Utilizing the periodicity of a SQUID's transfer characteristics in units of Φ_0, an n-b superconductor flash ADC uses only n clocked SQUID comparators [33]. To understand the periodicity, consider a single-junction SQUID [Fig. 3(a)] consisting of an inductor L_s and a junction J_0. The current through the junction is a periodic function [Fig. 3(b)] of the applied input current, with periodicity Φ_0/L_s. The basic comparator consists of a *flux quantizer* (single-junction SQUID) and a sampling circuit, called the

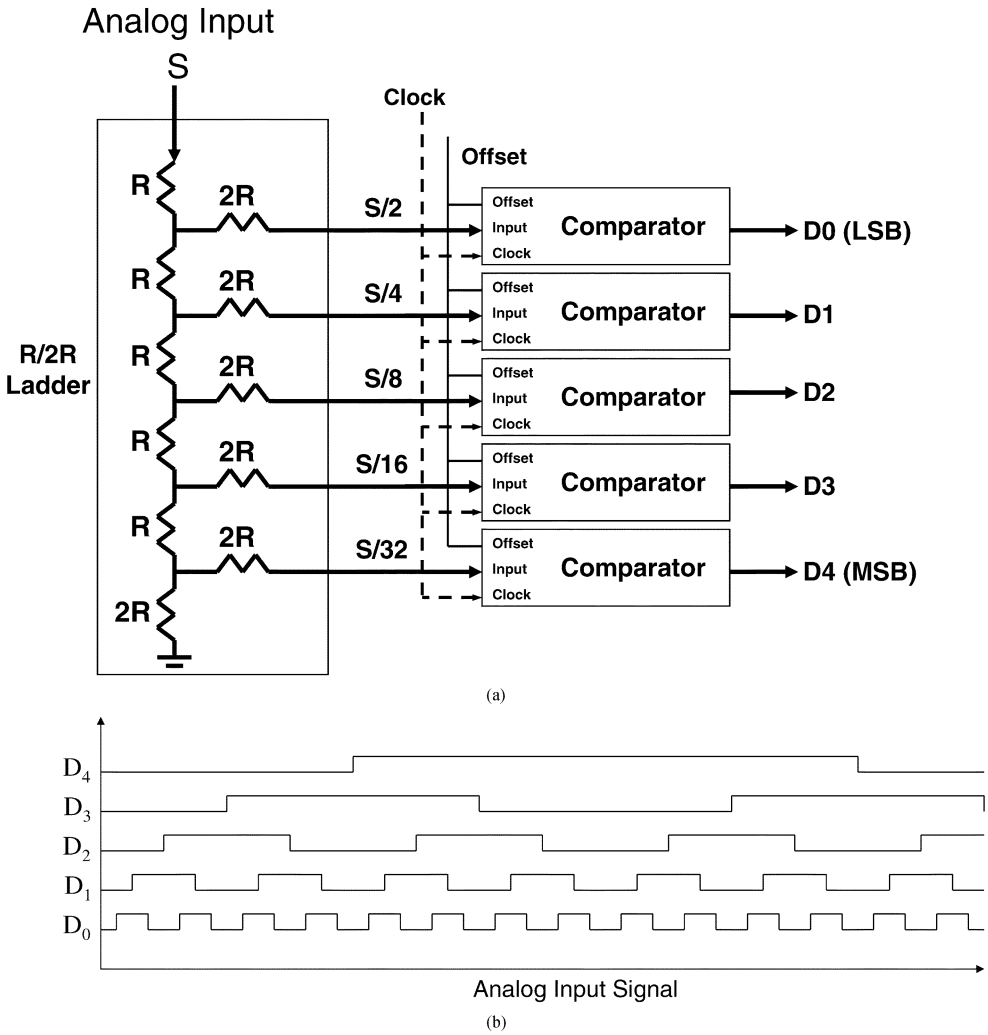


Fig. 4. Superconductor flash ADC with n SQUID comparators for an n-bit ADC. (a) Schematic diagram of a 5-b flash ADC showing the R/2R ladder and the periodic comparators. (b) Digital outputs of the ADC as a function of increasing input signal. Note that this is in Gray code, where only one bit changes at a time, reducing the likelihood of bit errors.

decision-making pair or balanced comparator, comprising two junctions in series [J_1 and J_2 in Fig. 3(c)]. When a clock signal is applied to the sampler, one of these two sampling junctions switches to the resistive state. For a clockwise current $I_{\rm loop}$, J_2 switches making the output a logical "1," whereas a counterclockwise current $I_{\rm loop}$ causes J_1 to switch producing a "0" output [Fig. 3(d)].

Fig. 4 shows the schematic of a flash ADC, producing an n-b digital Gray code. The input signal S is successively divided by factors of two and applied to a set of identical comparators, each with periodic thresholds [34]. The output of the first comparator is the least significant bit (LSB) and that of the last comparator is the most significant bit (MSB), encoded in Gray code. In an n-b ADC, the first comparator gets 2^{n-1} times the current applied to the last comparator. As the input signal increases, each comparator goes through multiple thresholds. Fig. 4 shows the digital outputs (D0–D4) of each comparator for linearly increasing input. Unlike standard binary code, in Gray code, only one of the output bits changes between consecutive digital numbers. Therefore, Gray code is less susceptible to errors due to slight misalignments of comparator thresholds.

Like all multicomparator ADCs, the superconductor flash ADC is susceptible to mismatched circuit components and conditions, such as the resistor ladder, delays in clock and signal paths, and, in this case, differences in local magnetic environment. Component mismatches depend on the quality of the IC fabrication process. For correct operation, the analog signal and the sampling clock must be applied simultaneously at each comparator, requiring precise transmission line designs on the signal and clock paths as they travel from the LSB comparator to the MSB comparator. This can limit the number of bits for a high-speed flash ADC. Still, three effective bits at $f_s = 20$ GHz have been experimentally demonstrated for junctions with $J_c = 2.5$ kA/cm^2 [4].

Threshold jitter affects the comparator only when the input signal is close to the threshold value. Unfortunately, it can sometimes cause catastrophic errors in a flash ADC, where the MSB receives the smallest amount of analog signal and, consequently, is the most susceptible to threshold jitter. This flaw can be corrected with a real-time digital error correction

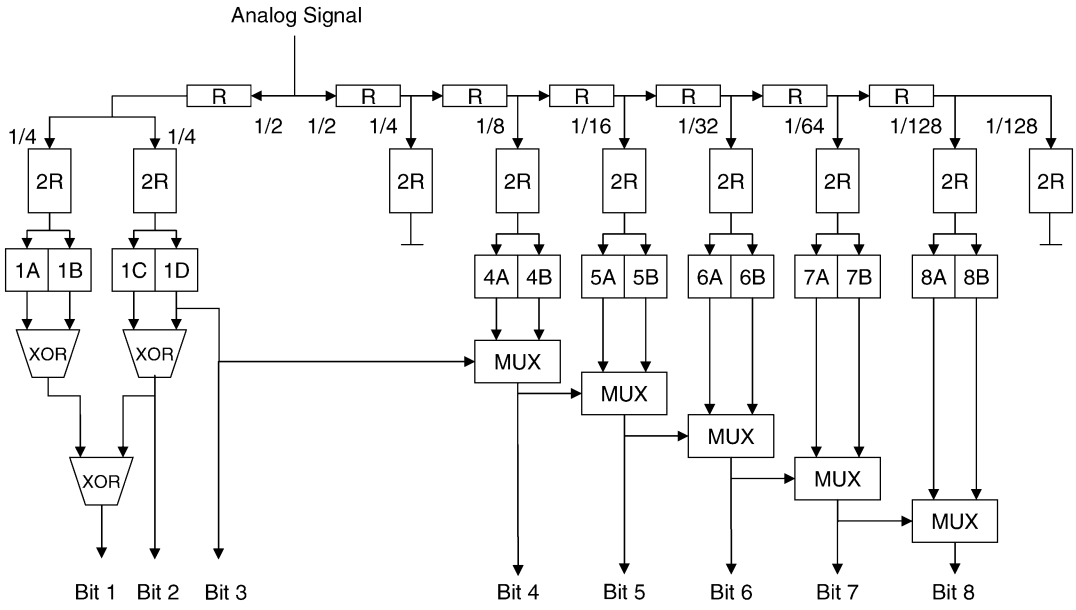


Fig. 5. Block diagram for an advanced superconductor flash ADC that includes redundant comparators and digital logic to correct ADC errors in real time [35]. Bits 1 and 2 are synthesized from a set of four comparators with interleaved thresholds and XOR real-time logic. Bits 4–8 each contain two comparators, and look-back digital error correction. This also converts the output from Gray code to standard binary.

technique [35], called the look-back algorithm [36], albeit requiring double the number of comparators. In this scheme, two comparators, offset from each other by a dc $\Phi_0/4$ flux bias, are used for each bit. This ensures that at most one comparator can be close to threshold for any input signal value. A two-input multiplexer (MUX) selects the comparator that is farthest from threshold based on the value of the previous bit (see Fig. 5). For bits 4–8, two comparators (A and B) are used and the output is chosen by selecting the B(A) output when the state of the previous bit is "1" ("0"). The look-back error-correction logic also converts the original Gray code output to standard binary. Furthermore, one can synthesize additional bits of lower significance by increasing the number of LSB comparators (as an example, Fig. 5 shows four LSB comparators) and successive exclusive-OR (XOR) operations. Synthesis of these additional effective bits is limited by the precision of timing and flux bias adjustments.

B. Superconductor Oversampling ADCs

Several distinctly different oversampling ADC designs were and are being developed using superconductor technology. These are various counting delta and sigma–delta type ADCs, phase modulation–demodulation (PMD) delta ADC, and conventional delta and sigma–delta ADCs. A majority of them are low-pass ADC designs, while recently, band-pass designs have increasingly become a center of interest especially for communication applications. While having quite different design approaches, most of them take advantage of the unique availability of implicit feedback and signal integration inherent to any SQUID loop. This is simply a consequence of conservation of flux in a superconducting loop; the SQUID loop automatically accumulates

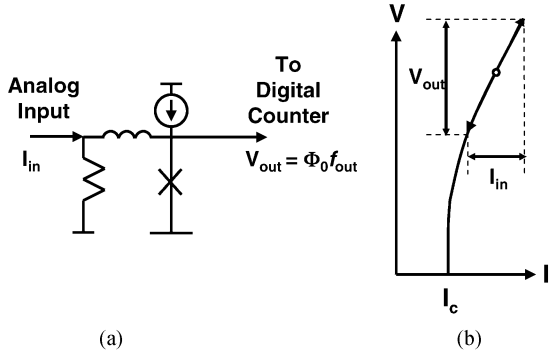


Fig. 6. Simplified V/F ADC modulator. (a) Equivalent schematic. (b) Approximately linear operating region.

the total flux with opposite sign (sum of antifluxons) of all SFQ pulses (fluxons) emitted by the Josephson junction.

1) Counting ADC (V/F ADC): Historically, the first Josephson ADCs [37], [38] were based on the voltage-to-frequency (V/F) conversion utilizing the ac Josephson effect. In this type of ADC, the processes of quantization and sampling are separated. A single Josephson junction [Fig. 6(a)] acts as a voltage-controlled oscillator (VCO) and produces an SFQ pulse train at a rate proportional to the applied analog voltage as $f = 2eV/h = V/\Phi_0$. This is a process of signal magnitude *quantization*. A very small shunt resistor converts input current to a voltage bias across the junction, with a tolerable range of linearity [Fig. 6(b)]. It is worth noting that there is an inductance (often omitted in diagrams) between the junction and the resistor which prevents the generated SFQ pulses from being shunted. This inductor also forms a SQUID loop (a resistive single-junction interferometer)

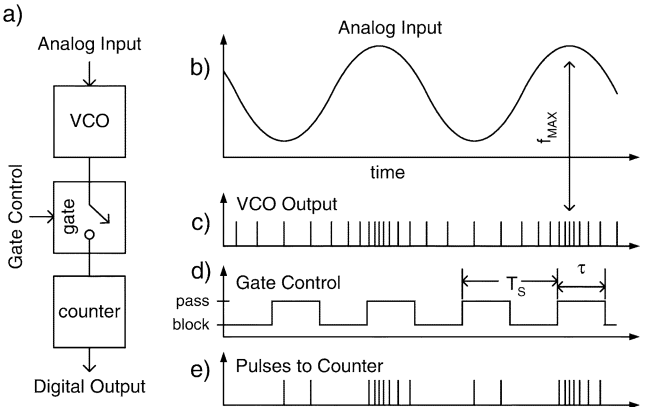


Fig. 7. V/F ADC. (a) Block diagram. (b) Input signal. (c) SFQ pulse output of voltage-to-frequency converter (VCO). (d) Gate control signals, with counting and sampling time intervals (τ and T_s) controlled by a fast RSFQ logic gate. (e) Resulting SFQ pulses sent to ripple counter [40].

allowing the realization of implicit feedback and integration functions.

The signal *sampling* process is performed by counting the number of generated SFQ pulses over a time interval (Fig. 7), which is controlled by a sampling gate. Overall, this analog-to-digital conversion is equivalent to a low-pass first-order sigma–delta modulation. The pulse counting process is done using toggle flip-flops forming a ripple counter, which are the fastest elements in RSFQ technology [20]. As a result, the digitized voltage averaged over the sampling period is read out from the counter. The exact analog between such a VCO-based circuit and a first-order low-pass delta–sigma modulator is derived in [39].

In order to avoid strong nonlinearities of such a VCO at low input signal, it is necessary to operate the VCO at some input offset. This offset also helps to accommodate positive and negative signals. A multijunction VCO was proposed in order to increase the resolution of the quantization process. It is based on interleaving of several single-junction VCOs while maintaining a fixed phase shift of one junction to another [40].

In order to increase the sensitivity of the V/F ADC, one can use a SQUID with a sensitive input transformer biased into the voltage state as a pulse generator [41], [42]. This transformer magnetically couples the input signal current (or flux) to a SQUID, which is biased above its critical current. The resultant flux in the SQUID loop produces modulation of the SQUID voltage. Once again, the SQUID produces an SFQ pulse stream, at a frequency that is exactly proportional to the voltage.

However, the periodic voltage-flux characteristic of the SQUID is nonlinear. One can extend the useful linear operating range by feeding a current proportional to the SQUID voltage back to the input (see Fig. 8). The SFQ pulse stream can be counted with an RSFQ digital counter to provide a digital count that is proportional to the integral of the applied current.

2) Counting ADC (Flux-Quantizing ADC): In another counting ADC design (flux quantizing or tracking ADC design) the input signal current is coupled into a SQUID loop, which generates one SFQ pulse for each Φ_0 change in flux [8], [43]–[45]. Similarly to the V/F ADC, these SFQ pulses can be counted using superconductor digital circuits to reconstruct the signal, with the precision limited only by the speed of the signal.

Let us consider the simplest configuration of a flux-quantizing ADC for a monotonically changing input signal. The input analog signal is transduced as a flux in a superconducting loop that includes a Josephson junction as switch [see Fig. 9(a)]. Each time the input increases the flux in the loop $(\Phi_{\rm loop})$ by Φ_0, the junction switches, creating a fluxon–antifluxon pair, one of which propagates as an SFQ pulse and the other decreases $\Phi_{\rm loop}$ by Φ_0. This automatic subtraction of the output signal from the input makes it equivalent to low-pass first-order delta modulation, where the output is differentially coded or proportional to the derivative $d\,\Phi/dt$ of the signal. The SFQ pulses can be counted over a time interval in a digital counter; each count corresponds to the change (rather than stationary value) of input signal in that interval. The sensitivity of the analog-to-digital conversion is set by the mutual inductance.

This concept can be expanded to accommodate both polarities of input signal derivative. Fig. 9(b) shows a scheme with two junctions, biased such that one of them switches when the flux in the loop changes by $+\Phi_0$ and the other when it changes by $-\Phi_0$, followed by bidirectional (up and down) counting implemented either using two counters [43] or a single bidirectional counter [8], [45]. In order to increase internal resolution of the SQUID quantizer, it is possible to use a "SQUID wheel" approach, in which a set of N interleaved quantizers are connected in parallel, so their thresholds are shifted by Φ_0/N [44]. One of the problems associated with the flux-quantizing ADCs is the hysteretic nature of the SQUID quantizer in response to changing polarity of the signal derivative.

3) PMD ADC: In order to solve the problem of the quantizer hysteresis, a dc voltage-biased single-junction SQUID quantizer (Fig. 10) was introduced [46]. The voltage source continuously pumps flux into a quantizer at a constant rate, where it adds to a flux induced by the input signal and then leaves the quantizer in the form of SFQ pulses via the only junction. In practice, the voltage source is implemented as a frequency-stabilized phase generator [47].

The basic concept of this delta ADC is illustrated in Fig. 11. The phase generator causes a SQUID quantizer to pulse at a rate which is modulated by the derivative of the incoming analog signal. This is essentially an encoding of the derivative into SFQ pulse positions. The modulated SFQ pulse train is passed to a synchronizer; a clocked sampling circuit generates a "1" or a "0" indicating whether or not an SFQ pulse arrived during that clock interval. It is possible to increase the resolution of this low-pass first-order delta modulation by using a multichannel synchronizer, which effectively subdivides the clock period [47]. Functionally, this multichannel synchronizer increases the number of quantization levels (m). The subsequent digital filter inte-

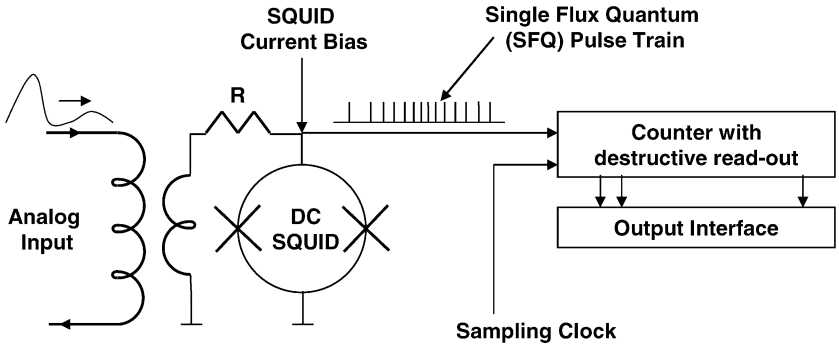


Fig. 8. Schematic of a sensitive V/F ADC based on the V-Φ transfer characteristic of the SQUID and followed by an RSFQ binary counter.

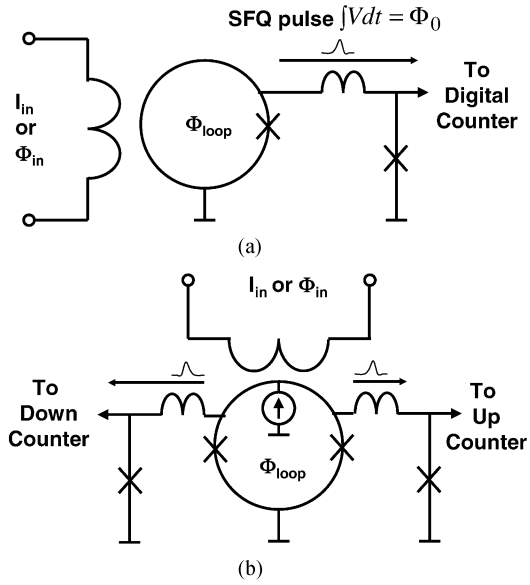


Fig. 9. Basic designs for counting ADC modulators, where analog signal current is inductively coupled into SQUID loop, and each change in flux by Φ_0 generates an SFQ pulse. (a) Basic unidirectional counting ADC modulator. (b) Basic bidirectional ADC modulator, with two counters or a single bidirectional counter.

grates the signal and averages it further, reducing the output bandwidth and increasing the ENOB.

Since this PMD ADC really measures the signal derivative, its maximum input is determined by a *slew rate limit* corresponding to a flux rate of $\Phi_0/2$ per clock period, of either sign. For a clock frequency f_s and a sinusoidal signal of frequency f_0, the maximum signal amplitude is $\Phi_{\max} = (\Phi_0/2\pi)(f_s/2f_0) = (\Phi_0/2\pi)\,R$, where R is the oversampling ratio. Before filtering, the LSB is $\Delta\Phi = \Phi_0/2m$. The corresponding unfiltered quantization error has an rms value of $\Delta\Phi/\sqrt{12}$, assuming a uniform (white noise-like) distribution between $-\Delta\Phi/2$ and $+\Delta\Phi/2$. The great advantage of oversampling is that subsequent low-pass decimation filtering narrows the noise bandwidth, which (for white noise) reduces the noise power level by the decimation ratio (N). Consequently, the value of the LSB scales down to $\Phi_0/2m\sqrt{N}$. Thus, the total dynamic range (DR),

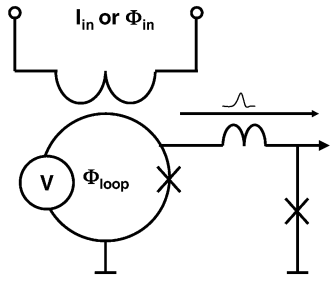


Fig. 10. Flux quantizer for phase modulation demodulation (PMD) ADC modulator.

from $-\Phi_{\max}$ to $+\Phi_{\max}$, in units of LSB, and the ENOB can be presented as

$$\mathrm{DR} = \frac{2\Phi_{\max}}{\mathrm{LSB}} = \frac{2}{\pi} mR\sqrt{N} = 2^{\mathrm{ENOB}}. \tag{2}$$

The SNR at the slew-rate limit is given by

$$\mathrm{SNR} = \frac{\Phi_{\max}^2/2}{(\mathrm{LSB})^2/12} = \frac{6}{\pi^2} m^2 R^2 N. \tag{3}$$

To take full advantage of oversampling, one must decimate all the way down to the Nyquist sampling rate $2f_0(N = R)$ and obtain the optimum value of the signal-to-noise power ratio $(6/\pi^2)m^2R^3$. The R^3 dependence of the SNR, varying at 30 dB/decade or 9 dB/octave, corresponds to a first-order oversampling ADC. By changing the decimation ratio N, usually by factors of two, one can trade off bits of resolution (ENOB) versus bandwidth $(f_s/2N)$ at a rate of 1.5 b/octave.

For example, if $f_s = 10$ GHz and $f_0 = 10$ MHz, the SNR with $m = 2$ is 3×10^8, or 85 dB corresponding to an impressive 13.8 effective bits. The measured performance was found to follow this trend, although apparently with a small amount of extra noise referenced to the input (see Fig. 12). Note that since both SNR and SFDR are linear with input signal up to saturation, both noise and spur levels are essentially independent of signal level. This indicates that this ADC is extremely linear over its entire range, unlike many conventional ADCs which generate increasing nonlinear distortion as saturation is approached.

This PMD ADC was fabricated (Fig. 13) and extensively evaluated, including a complete digital filter integrated on the

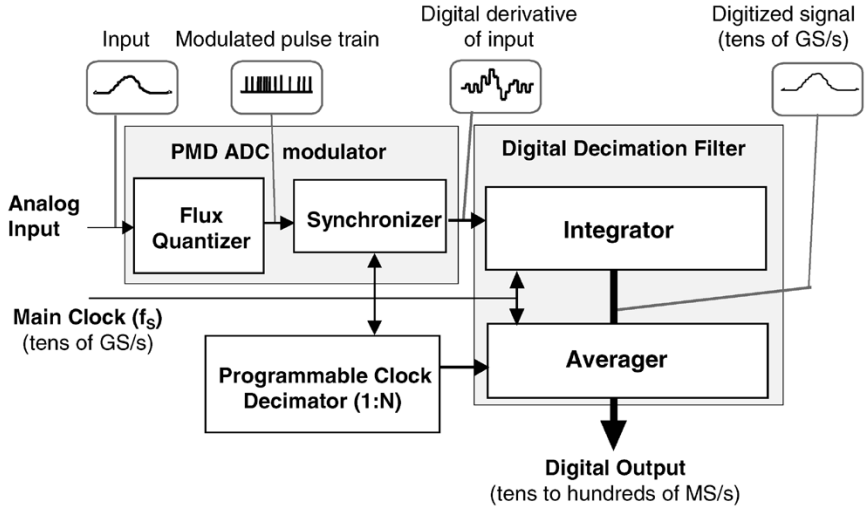


Fig. 11. Block diagram of the PMD ADC. The signal is inductively coupled to a voltage-biased quantizer, which acts as an SFQ pulse position modulator. The pulse train is synchronized to generate a differential digital code for the signal, which is subsequently integrated and averaged in an on-chip digital decimation filter. The final output at a reduced sample rate set by an on-chip programmable clock decimator is transmitted to room-temperature electronics.

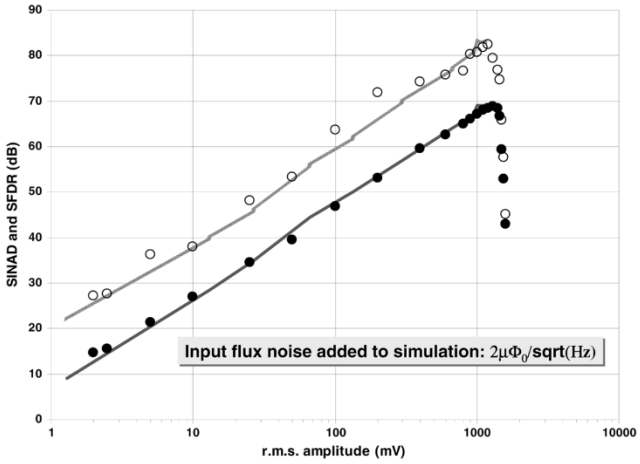


Fig. 12. Comparison of measured (circles) and simulated data (lines) for SNR (bottom data set) and SFDR (top data set) for the PMD ADC chip running at 11.2-GHz clock rate, 175-MS/s output sampling rate (factor of 1 : 64 decimation), and 10-MHz input sine wave. In order to achieve a close fit, an input flux noise of $2\,\mu\Phi_0/\sqrt{}$ Hz was added [50].

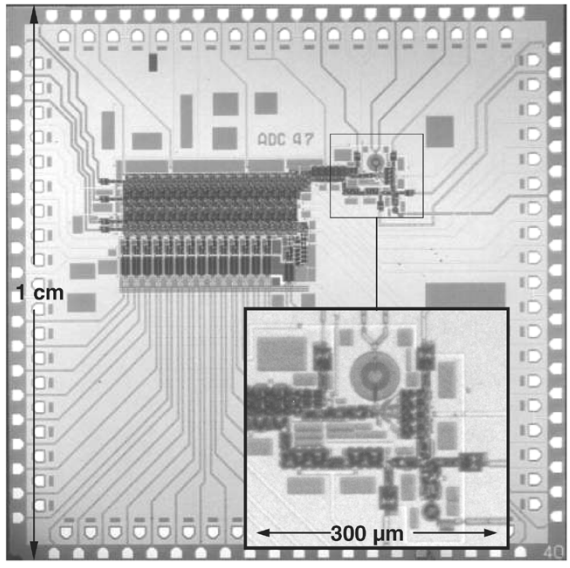


Fig. 13. 15-b ADC chip consisting of low-pass PMD delta modulator (in the inset) and decimation digital filter operating at 19.6-GHz clock. The 10 mm × 10 mm chip contains about 6000 Josephson junctions [50]. The large input transformer shown in the inset increases the ADC sensitivity. An external sinewave is applied to a smaller transformer at the bottom to generate clock SFQ pulse train.

same chip [5], [48]–[50]. The ADC performance was measured for various input single-tone and two-tone sine waves. The single-tone results are plotted in Fig. 2 in comparison to the state-of-the-art ADCs. The resolution/bandwidth tradeoff was measured at 1.45 b/octave, which is close to the theoretical value of 1.5.

4) Delta ADC: All oversampling ADCs described above are built with *quantization* and *sampling* processes performed by separate circuits. Fig. 14 shows a delta ADC modulator, in which these processes are performed *simultaneously* using a synchronous quantizer based on clocked comparator J1, J2. This low-pass delta modulator has two feedback loops and two integrators: an implicit loop due the conservation of magnetic flux in the superconducting loop of the quantizer and an explicit loop formed with the Josephson vortex transistor and a low-pass filter [51], [52].

Fig. 15 shows a complete ADC chip with the delta modulator including a decimation digital filter. It was fabricated using a standard 1.0-kA/cm^2 process and demonstrated its operation at up to 10.5-GHz clock. Although the modulator in Fig. 14 has two loops, its performance corresponds to that of a first-order modulator. In order to improve its performance closer to the second-order characteristics, it is necessary to increase gain in the explicit feedback to compensate losses in resistor R_F. This can be done by

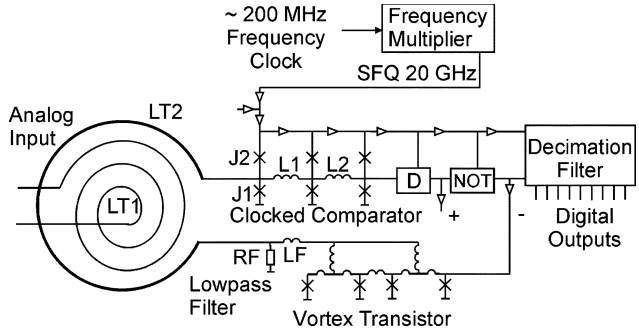


Fig. 14. Delta ADC based on a synchronous quantizer [52].

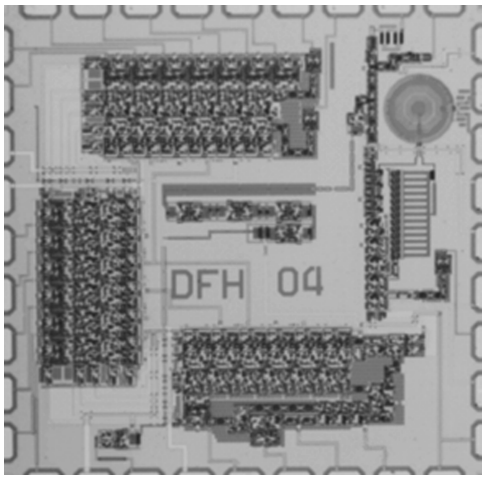


Fig. 15. Delta ADC chip consisting of low-pass delta modulator and decimation digital filter. The digital filter is broken into three parts connected using passive microstrip lines in order to fit into a 5 mm × 5 mm chip [52].

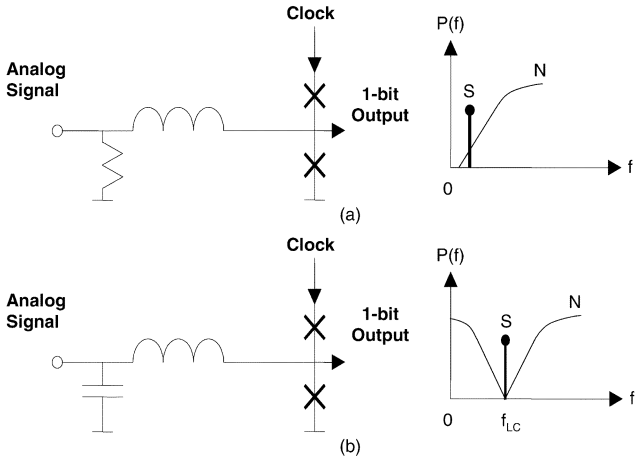


Fig. 16. Superconductor first-order sigma–delta modulators with implicit feedback. (a) Schematic of low-pass modulator, with input LR integrator, showing noise suppression at low frequencies. (b) Schematic of band-pass modulator, with input LC filter, showing noise suppression around resonant frequency f_{LC}.

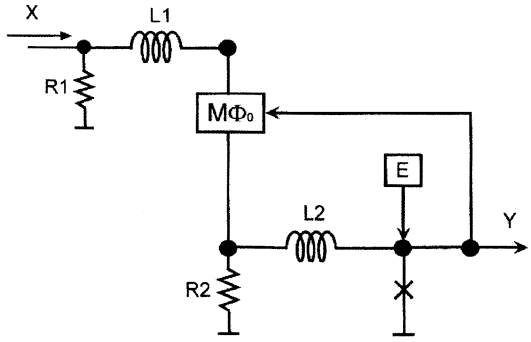


Fig. 17. Superconductor second-order sigma–delta modulator [60].

replacing the vortex transistor with amplifiers [53] based on voltage multiplier circuits [54], [55]. With a gain of eight, its performance will be somewhat higher than the first-order modulator [53].

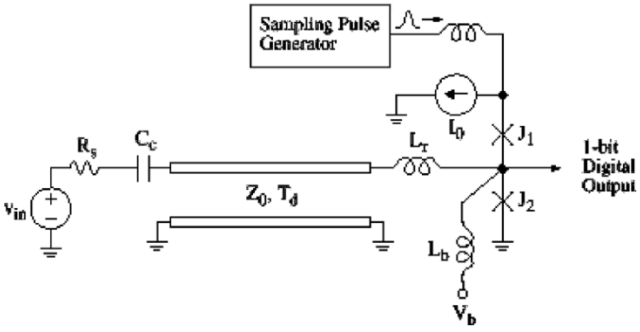
5) Low-Pass Sigma–Delta ADC: The synchronous quantizer can also be used to build a conventional low-pass sigma–delta ADC modulator by adding an analog LR integrator in front. It is known that a first-order sigma–delta modulator is functionally equivalent to a delta modulator preceded by an integrator [24]. Similarly to the delta ADC modulator described above, *quantization* and *sampling* are performed *simultaneously*.

The simplest circuit design for a Josephson first-order low-pass sigma–delta ADC is shown in Fig. 16(a) [56]. Again, the feedback is implicit due to the flux conservation of the superconducting loop. This does indeed exhibit suppressed noise at low frequencies, as shown in the power spectrum to the right of the circuit. It is important to note that because of the quadratically rising noise, a simple first-order decimation filter is insufficient to filter out the high-frequency noise; at least second order is necessary. It is possible to build a first-order sigma–delta modulator with an explicit feedback using digital-to-analog circuits. However, this modulator design has higher complexity with similar anticipated performance [57].

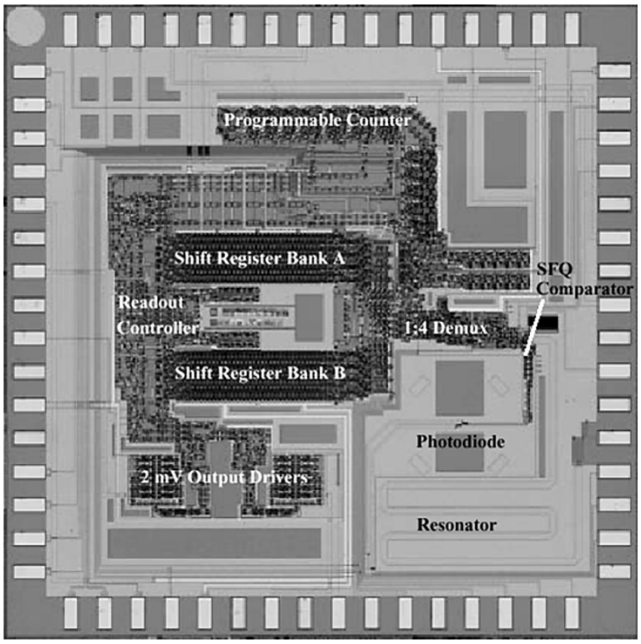
Due to the relative simplicity of the first-order modulator design with implicit feedback, it was implemented using both LTS [58], [59] and HTS materials [29]–[32]. Since no on-chip digital filter was implemented, modulator performance was measured directly with an analog spectrum analyzer. The first-order modulator demonstrated SFDR $= 78$ dB (13 SFDR bits) for a 5-MHz signal [58].

The second-order modulator design is capable of increasing the ADC performance substantially [see (1)] improving SNR from 9 to 15 dB/octave of oversampling. Fig. 17 shows a two-loop modulator design employing an explicit feedback in addition to the existing implicit one [60]. Similarly to the previously described delta modulator, signal losses in R2 require providing a substantial gain (M) in the explicit feedback. There have been several attempts to realize this challenging amplification task, which has to deliver enough gain $(M \sim 64)$ within a very short time, below the high-speed clock period [61]–[64]. The most sophisticated amplifier based on a magnetically coupled Josephson transmission line (JTL) tree and serially connected SQUIDs demonstrated close to 12-dB/octave power spectrum characteristics although at a relatively low 1.2-GHz clock rate [64].

6) Band-Pass Sigma–Delta ADCs: Replacing the front-end LR integrator with an LC resonator as shown in



(a)



(b)

Fig. 18. Superconductor first-order band-pass sigma–delta ADC based on microstrip resonator [69]. (a) Schematic of sigma–delta band-pass modulator. (b) 6.3 mm × 6.3 mm test ADC chip incorporating the band-pass modulator and digital data buffers with 4065 Josephson junctions.

Fig. 16(b) will convert a low-pass modulator design into a band-pass design [65]. It suppresses the quantization noise around the resonant frequency f_{LC}, rather than at dc. Superconductor technology is particularly suitable for implementing band-pass ADC designs. There are two major advantages: low-loss materials allowing very high Q of resonators and high clock rates allowing direct sampling of multigigahertz RF signals.

This was demonstrated with the realization of superconductor first-order sigma–delta ADC modulators, where both a lumped LC resonator [66] and a microstrip resonator have been used (Fig. 18) [67]. With the microstrip resonator, this has been demonstrated up to a sampling rate of 45 GHz and was found to exhibit the desired suppression in noise around the center of a band at 2.2 GHz, as well as at higher harmonics of this resonance [68], [69]. The demonstrated performance (SNR of 49 dB and dynamic range of 57 dB over ∼20 MHz bandwidth at 2.2 GHz) exceeds that of semiconductor band-pass modulators.

C. Superconductor Multimodulator ADCs

Challenges in building higher order modulators and/or increasing their clock frequency encourage development of alternative approaches to increase ADC performance. Several such approaches are known in conventional semiconductor ADC technology: time-interleaving, subranging, cascading, and others. Likewise, these techniques can be utilized in superconductor technology.

1) Time-Interleaved ADC: Time interleaving allows the increase of effective sample rate by using several parallel comparators sampled by the same clock. The actual performance gain in the interleaved oversampling ADC depends on various factors, including delay in the feedback loop in comparison to the effective clock period. Fig. 19(a) shows a block diagram of a time-interleaved delta modulator consisting of two delta modulators shifted by half a clock period [70], [71]. Interleaving of the modulators requires interleaving both comparator and feedback functions. This cannot be achieved with the implicit feedback of SQUID quantizers, in which comparator and feedback function are combined. Fig. 19(b) shows "nondestructive comparators" with suppressed feedback function. Instead, a separate explicit feedback loop is implemented using stacked SQUIDs [70]. The interleaved modulators were integrated with an on-chip digital filter designed to process the interleaved data streams [Fig. 19(c)].

2) Subranging ADC: Subranging allows one to increase dynamic range by using several modulators to digitize different ranges of signal amplitude. A simple two-stage subranging architecture was implemented for a digital SQUID [72]. This approach can also be extended for a band-pass sigma–delta ADC (Fig. 20). The first "coarse" band-pass modulator performs an initial digitization of input signal. The digital output is then converted back to analog form using a linear single-bit DAC followed with analog band-pass filtering. The resultant signal is subtracted from the appropriately delayed input signal. The difference is then applied to the second "fine" modulator. The following DSP combines both coarse and fine outputs to form an ADC output [73]. The most challenging part of a subranging ADC is the accurate matching of the subtracted signals in gain and time delay.

III. Related Superconductor Circuits

Any complete digitizing system requires a number of additional circuits to be integrated on the same chip with the ADC modulators. These are digital circuits to reduce digital data rate, perform filtering and processing of the data (demultiplexers, memory buffers, digital decimation filters, digital downconverters, and local oscillators), and support the analog-to-digital conversion process (clock sources, clock controllers, output drivers, etc.). There is also an emerging class of digital RF processing circuits performing digital signal processing on high-data rate and low-bit-width output of ADC modulators. In this section, we focus only on two critical examples: decimation digital filters and on-chip clock sources.

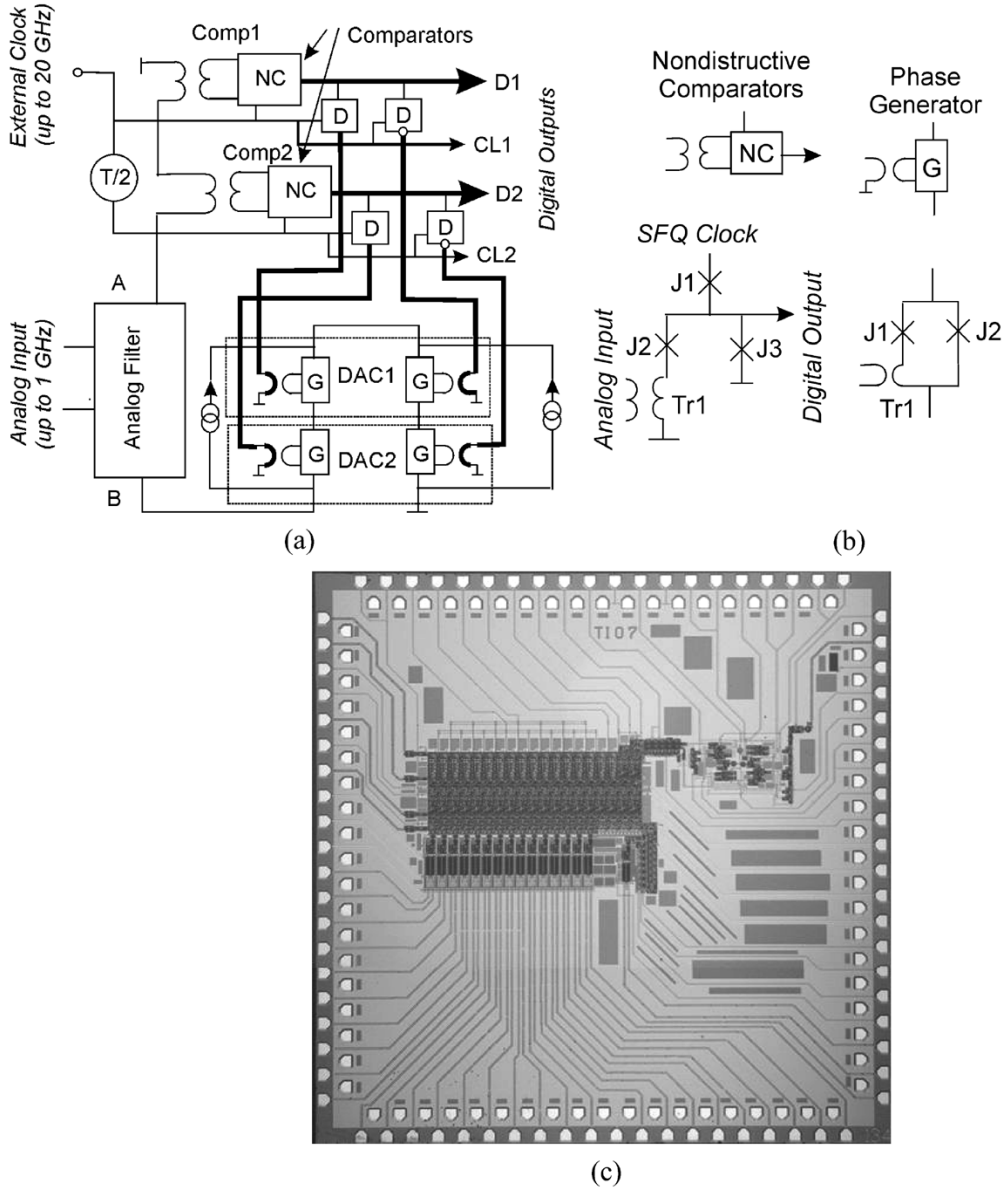


Fig. 19. Superconductor two-channel time-interleaved low-pass delta ADC [70]. (a) Block diagram of the ADC modulator. (b) Notations and equivalent circuits of basic modulator components. (c) 5 mm × 5 mm ADC chip incorporating the modulator and a decimation digital filter.

A. Digital Decimation Filters

An oversampling ADC with a one (or a few) bit modulator is incomplete without a digital decimation filter that reduces the sampling rate, narrows output bandwidth, and generates additional bits. A common approach to such filters, originally due to Hogenauer [74], is known as comb, sinc, or cascade–integrator–comb filtering (CIC). For the case of superconductor ADCs, sinc-type filters have to be implemented using ultrafast RSFQ logic due to very high modulator output data rates (tens of gigahertz). Since both ADC modulator and digital filter are built using the same low-power RSFQ technology, it is quite straightforward to integrate them on the same chip without any digital signal interference problem common in semiconductor mixed-signal IC design.

The basic concepts are illustrated in Fig. 21 for a delta modulator and a delta–sigma modulator. In the former case [Fig. 21(a)], after integrating the 1-b data in an accumulator (essentially a binary counter), the output (still at the full clock rate f_s) is decimated by a factor of N by summing (averaging) and reducing the output rate to f_s/N. This averaging is equivalent to a sinc filter, with an out-of-band rolloff envelope of 6 dB/octave. For example, an initial rate of 20 GHz can be reduced by a factor of 256 to an output rate of ∼80 MHz, which can then be processed further by conventional electronics [5]. One of the important features of superconductor ADCs is the possibility to trade output sample rate (i.e., signal bandwidth) for resolution using a dynamically programmable clock prescaler which sets the level of averaging and the output sample rate. This prescaler is integrated into the filter and allows instant reprogramming during its

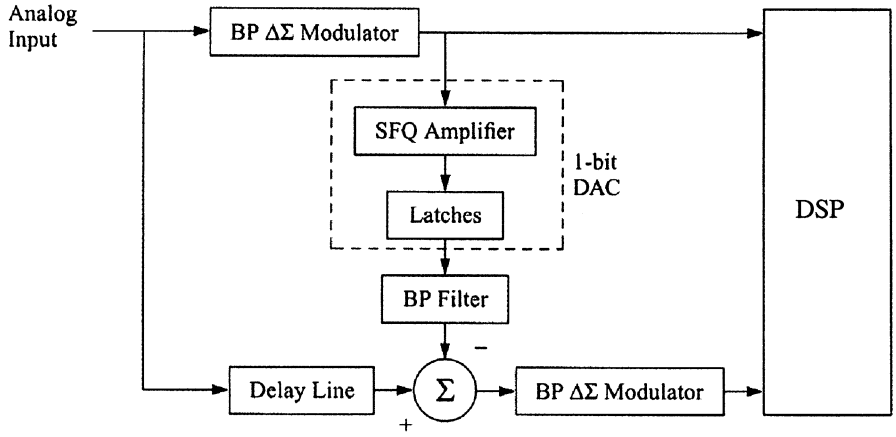


Fig. 20. Suggested subranging architecture for superconductor band-pass sigma–delta ADC [73].

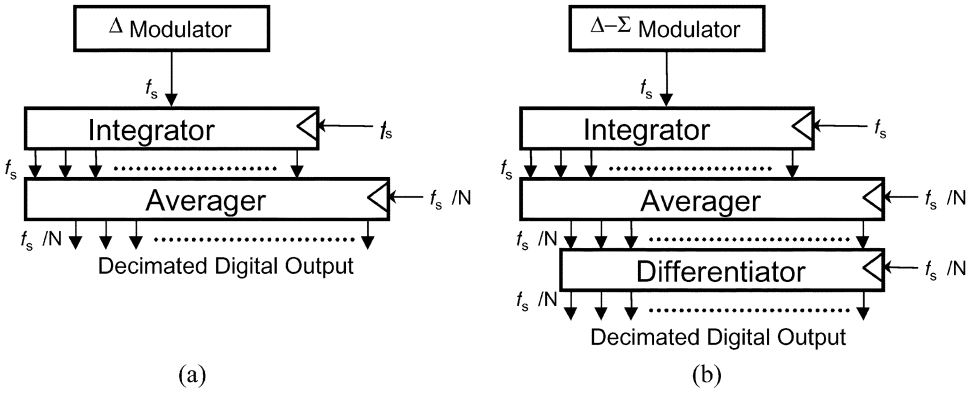


Fig. 21. Block diagrams of basic decimation filters for superconductor ADCs. (a) Integrator (accumulator) reconstructs the signal from a delta modulator, then a first-order sinc filter (averager) generates the decimated output. (b) Second-order (sinc^2) filter for first-order delta–sigma modulator, with sequential integration in an accumulator, decimation in an averager, and differentiation to recover the decimated signal.

operation using external controls. As a result, a single ADC chip is capable of instantly changing its bandwidth (within the front-end cutoff frequency) to zoom in or zoom out on some particular bandwidth of interest [5].

The digital filter architecture for a first-order delta–sigma modulator is very similar [Fig. 21(b)]. An accumulator is followed by an averager, and the decimated input signal is recovered using a subtractor (differentiator). This is equivalent to a sinc^2 filter, which has out-of-band rolloff of 12 dB/octave, sufficient to filter out the rising high-frequency quantization noise of the delta–sigma modulator. This differentiator operates at f_s/N, so that it can generally be carried out at room temperature using conventional electronics. This reduces the complexity of the superconductor ADC chip.

This approach can also be generalized to higher filter orders. Each higher order requires one additional accumulator on the front and differentiator at the back end. For example, a sinc^3 filter (which would be required for a second-order delta–sigma modulator) would have two accumulators on the front and two differentiators at the back, with a decimating averager in the middle. A modular filter design has been developed to facilitate the synthesis of higher order filters [75].

RSFQ digital technology, fundamentally built on elementary latches (flip-flops), is particularly convenient to implement high-throughput, bit-pipelined digital filters [51], [53], [75]–[78]. Besides ubiquitous D flip-flops, just two types of RSFQ cells, toggle flip-flop with destructive (TD) and nondestructive (TN) readout, form a basis for the filter design. An addition of half-adders allows the enlargement of critical timing margins and speeding up of the filters [75].

Simple prefilter RSFQ encoders can extend the basic filter structure to accommodate multichannel input data, e.g., data streams from a time-interleaved ADC [75], [76] or from the multichannel synchronizer of a PMD modulator [47], [48].

B. Digital Clocks

The reduction of timing jitter is very important for the ADC sampling clock, since jitter directly affects the conversion accuracy. In RSFQ ADC technology, a common master clock signal is typically used for both ADC sampling and for clocking of digital circuits on the same chip. The required clock frequency is in tens of gigahertz for the current superconductor IC fabrication technology and is expected to increase to hundreds of gigahertz as the technology matures. Typically, the required clock signals, in the form of a periodic

sequence of SFQ pulses, are derived from an external oscillator (e.g., an Agilent sinewave generator) using a standard dc/SFQ converter circuit [5]. To maintain the expected ADC performance enhancement as a function of increasing clock frequency, the clock jitter must decrease proportionately. It is possible to increase the SFQ clock frequency using on-chip frequency multipliers based on SFQ mergers [51]. However, it becomes increasingly difficult to achieve sufficiently low jitter at higher frequencies when deriving the clock from external, noncryogenic oscillators.

Another possibility is to utilize an optical sampling technique converting low-jitter optical pulses into SFQ pulses with a metal–semiconductor–metal photodetector (MSM diode) integrated on the ADC chip [68], [69], [73]. Perhaps, it can eventually be made into a practical and compact system.

Superconductor electronics offers a variety of on-chip oscillators that can produce high-frequency clocks for ADCs and other digital circuits. The simplest clock generator is a single-junction VCO employing the ac Josephson effect. When a dc voltage V is applied to the junction, the junction oscillates at a frequency $f = V/\Phi_0$. Since the voltage required for the 20–100-GHz frequency range is low (40–200 μV), the voltage noise across the bias resistor, and consequently the clock jitter, can be significant. One of the critical design issues with such a clock source is the jitter degradation in the VCO loaded with a Josephson transmission line. It is also possible to use an array of junctions to reduce the spectral linewidth and increase oscillator output power. Both single-junction and array oscillators are advantageous to generate $>$100 GHz frequencies.

For lower frequencies, ring oscillators formed by segments of Josephson transmission lines have been used [79], [80]. Another approach is to use a long Josephson junction (LJJ) oscillator, either in the flux-flow mode or in the soliton resonance mode. RSFQ clock sources using linear and annular LJJ oscillators have been demonstrated in the 10–50-GHz range [81], [82]. These oscillators have very narrow linewidths, with quality factors $(Q = f/\Delta f)$ in the 10^5–10^6 range and very low timing jitter ($\sim$50 fs) [83], [84].

A system incorporating a band-pass ADC will also require a digital local oscillator for the digital downconverter (mixer) to shift the signal band down to baseband. As for the sampling clock, such an oscillator can either be introduced externally or else synthesized on-chip. For example, an on-chip oscillator may be easily obtained from submultiples of a master clock.

In order to ensure long-term stability and synchronization with an entire system including room-temperature electronics, an RSFQ phase-locked loop (PLL) circuit has to be used [85].

IV. Applications and Future Prospects

A. Digital Communications

Perhaps the biggest ADC application area dominating the research and development funding and industrial efforts in recent years has been the wireless commercial and defense communications and related technologies in the radar and electronic warfare sectors. These applications have in common the requirement of directly digitizing RF signals, with gigahertz sampling and high dynamic range ($>$14 b). These processes are now done using one or more steps of analog mixing and amplification, which introduce excess nonlinearity and noise into the signal. Conventional technology requires a separate analog receiver and transmitter for each such protocol and subband. In contrast, a *software (defined) radio* (SDR) system could include a single universal receiver and transmitter (or "transceiver"), with all of the special-purpose processing being done digitally [86], [87].

However, practical realization of the SDR presents a multitude of technical challenges. The wide bandwidth requirement means that such a transceiver will be left open to a large number of carriers, potentially creating an overlapping picture of cochannel interferences, aliases, and intermodulations. The requirement of simultaneous handling under software control of a large number of signals with different coding, protocols, hopping patterns, etc., implies that the inflexible analog front-end components would be replaced by very high speed digital parts bringing the digital domain as close to the antenna as possible.

To meet these requirements, a true SDR transceiver needs mixed-signal and digital components capable of delivering extreme speed, linearity, dynamic range, noise, and sensitivity. Neither conventional ADCs and DACs nor conventional DSPs have the necessary performance. On the other hand, the unique features of superconductor electronic technology lead to ultrafast circuits with the performances that can make a true SDR possible [59], [88], [89].

A novel "digital-RF" approach was introduced [89], [90], meaning performing data conversion and digital processing at RF rather than at conventional baseband. In this approach, the analog filter and up/down-conversion stages from/to lower IF or baseband are eliminated. The digital-RF architecture is illustrated in Fig. 22 using an example of a receiver. A wide-bandwidth RF signal is applied directly to an ADC modulator producing an oversampled low-bit-width digital code at very high data rate (tens of gigabits per second). This high-rate data stream is processed before down-conversion using a relatively low-complexity but very high-throughput processor, an RF DSP, to implement various functions such as digital signal combining from multiple channels, true-time delay for digital beamforming, adaptive active cancellation of transmit channels, correlation-based digital filtering, etc. Finally, this high-rate data is down-converted to baseband using digital mixers and decimation filters for further processing and decoding. Clearly, such an architecture can be realized only if both ADC and DSP can deliver sufficient performance and can operate at a very high clock rate (e.g., 20 or 40 GHz).

The digital-RF design principle can be extended to a whole transceiver (Fig. 23). The transceiver is clocked with an integrated low-jitter high-speed SFQ clock and synchronized with an external low-speed (10 MHz) reference clock using

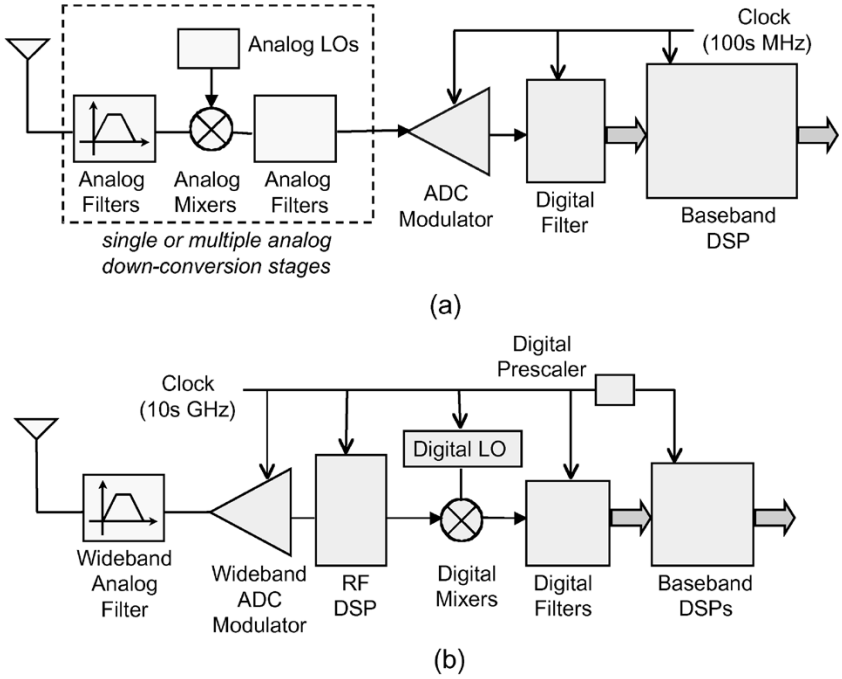


Fig. 22. Comparison of: (a) conventional and (b) digital-RF receiver architectures. In the digital-RF scheme, data conversion is carried out directly at RF frequencies using a wideband ADC modulator with large oversampling. The digitized RF low-bit-width data are then processed at very high data rates in an RF DSP before being digitally down-converted and filtered to baseband for further processing [90].

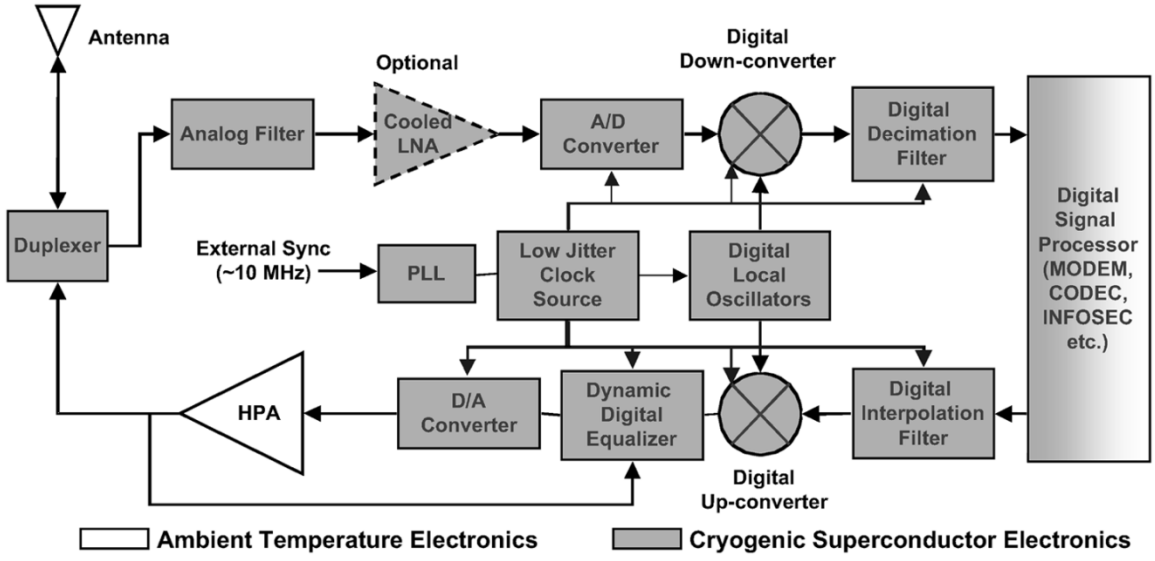


Fig. 23. Block diagram of a digital-RF transceiver, where data conversion is carried out directly at RF frequencies, and signal processing is done using ultrafast superconductor digital RSFQ circuits operating at tens of gigahertz (e.g., 20 or 40 GHz) [90].

a PLL. In the receiver chain, the RF signal from the antenna is filtered, (possibly) amplified, and then sent directly to an ADC. The down-conversion is carried out digitally, in a way that can be easily reprogrammed. A digital decimation filter is used to decrease the output bandwidth, while increasing the ENOB. This can be a quadrature receiver or be channelized into multiple baseband channels [91].

The transmitter part carries out the same digital functions in reverse. A fast DAC is clocked by a high-speed SFQ clock and generates spectrally pure RF signals to be amplified by a high-power amplifier (HPA). The diagram also shows a dynamic digital equalizer, a digital predistortion module, which is combined with the DAC to compensate for nonlinearities in the HPA. Since multiple channels can be combined digitally into one broadband digital-RF signal before amplification, only a single multicarrier HPA is needed.

All fast digital and data conversion processes shown in Fig. 23 will be carried out using RSFQ low-temperature superconductor (LTS) circuits cooled to cryogenic temperatures ∼4 K, as indicated by shading in the figure. The analog

filtering and duplexing can be carried out at an intermediate cryogenic temperature (∼60 K) in order to minimize thermal noise. The HPA and back-end processing will be implemented using conventional semiconductor parts and placed at ambient temperature. This hybrid configuration is compatible with available commercial cryocoolers, which employ two or more different temperature stages.

B. Ultrafast Instrumentation

There are several important areas of scientific and commercial instrumentation in which the precision, speed, and dynamic range of superconductor ADCs are of great interest. One such application is a transient digitizer with application to nuclear and high-energy physics [4]. Another application is a digital high-speed readout of a superconductor–insulator–superconductor (SIS) mixer for radio astronomy spectroscopy. The SIS digital readout can be implemented using a flash ADC approach [92] as well as a sigma–delta-type ADC based on a unique signal-to-delay transducer with race arbitration [41].

A transient digitizer (Fig. 24) is needed to capture nonrecurring ephemeral events. It is based on a superconductor flash ADC, combined with fast RSFQ logic and memory circuits to reduce the high output data rate. A prototype transient digitizer instrument, comprising a superconductor IC [Fig. 24(b)] along with a room-temperature interface and data acquisition electronics, was demonstrated for single-shot pulse capture [4]. Each digitizer circuit contains a 6-b flash ADC, which is coupled to a bank of 32-stage shift registers through a set of acquisition control switches. Fig. 24(c) shows the results of a pulse capture experiment with the 6-b digitizer chip. For a practical system, it would be necessary to have an ADC calibration circuit (a silicon DSP) to accurately set up all thresholds and biases, similar to systems employing semiconductor flash ADCs.

A multichip digitizer, with the flash ADC on one chip and several modular memory chips, may be required to address the longer acquisition memory requirements for some applications. This modular design requires fast interchip connections for data and clock signals between the flash ADC and the shift register, which has been demonstrated up to 10 Gb/s [93]. The interchip data transfer can be extended to 60 Gb/s [94].

Multichannel time digitizers [time-to-digital converters (TDCs)] have also been demonstrated using RSFQ circuits and a simple front-end SQUID quantizer [21]. These have application to collision and decay measurement in high-energy particle accelerators, where picosecond timing precision between multiple events is necessary. Such time resolution follows naturally from the multigigahertz clock rates of RSFQ circuits. Systems demonstrated include an 8-channel multihit TDC with 30-ps resolution (fabricated on a single 1-cm chip containing 10 000 Josephson junctions), a two-channel 6-ps TDC, and a dual-function multihit TDC/ADC, which provides pulse amplitude information as well as timing. Even finer timing measurement is anticipated as clock rates are further increased by scaling to smaller Josephson junctions.

C. Sensor Readout

Low noise, low power, high sensitivity, and radiation hardness of superconductor ADCs are of prime importance for many sensor technologies, especially for cooled detector arrays.

The NbN 10 K V/F type ADC was demonstrated for cryocooled IR focal plane detector arrays [28]. A Nb 4 K 16-b PMD delta ADC with serial optical fiber output to minimize heat load was developed for IR array readout [95].

Another Nb 4 K V/F type ADC with a SQUID-based VCO was used for measuring the integrated charge of a current pulse for superconductor tunnel junction (STJ) X-ray detector readout. Furthermore, the same digital counter can be used to count the number of SFQ clock pulses between successive time events to produce a TDC on the same chip. Such a dual-function signal and time digitizer was recently demonstrated with 1-μA full-scale current and 30-ps time resolution [41], [42].

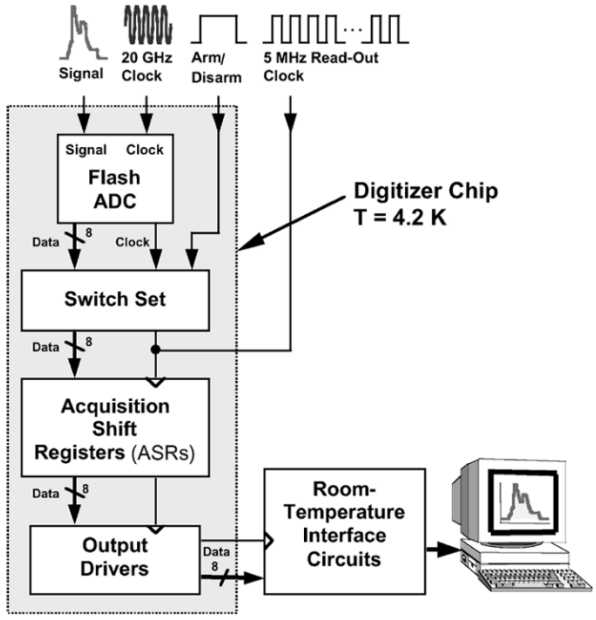
The exceptionally low power of RSFQ technology allows integration of an ADC or TDC in a single cryopackage with the cooled detectors. The integration of the cooled semiconductor detector, visible light photon counter (VLPC), was demonstrated with a single-hit TDC chip equipped with a sensitive SQUID-based V/F ADC [96].

The extreme radiation hardness of superconductor electronics was a motivation for the readout of a high-energy particle microstrip detector. In this design, a simple delta ADC based on a very sensitive flux-controlled comparator was demonstrated [97].

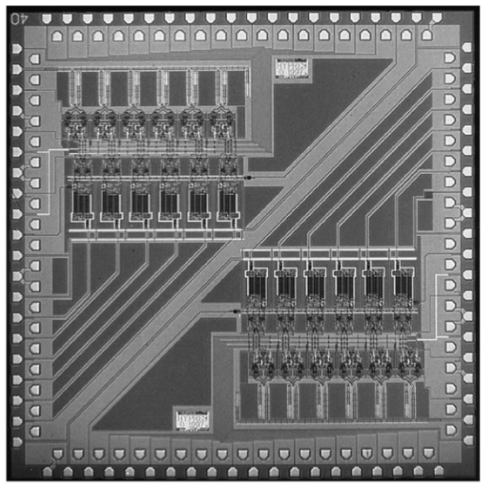
Digital SQUID magnetometers [98]–[100] undoubtedly deserve special treatment. They are essentially high-sensitivity low-noise ADCs with a very high dynamic range. Their design is close to that of oversampling ADCs. Their specific design features, development milestones, and trends are beyond the subject of this paper.

V. Conclusion

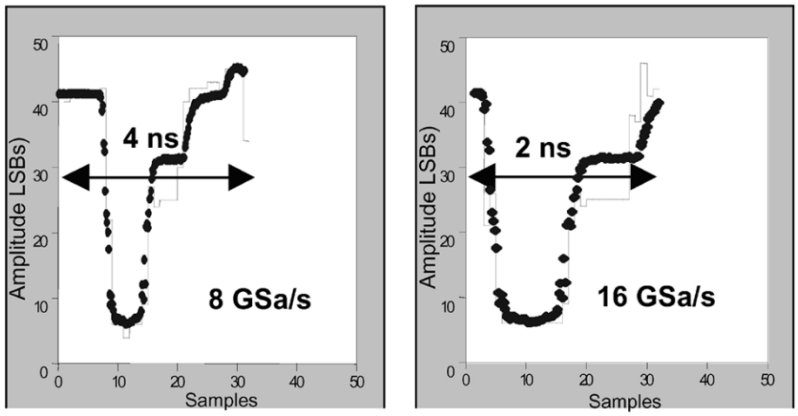
A wide variety of superconductor ADCs have been developed over the past decade, combining ultrafast speeds of Josephson junctions with the quantum precision of magnetic flux quantization. These have demonstrated excellent performance in the laboratory, in both bits and bandwidth, for both Nyquist-sampling and oversampling ADCs. Over time, ICs with these ADCs have increased in complexity, including error correction and digital filtering. Complete prototype systems are being developed for challenging applications in communications, fast measurement, and sensor readout. They include cryocoolers (closed-cycle refrigerators) and automated room-temperature interface hardware and software. In the near future, it is expected that smaller Josephson junctions, higher levels of circuit integration, and more sophisticated circuit designs will lead to even higher speeds and greater dynamic range. For example, true digital-RF processing of broad bandwidths of multigigahertz signals should be feasible, enabling further application to such new technologies as software-defined radio and digital radar. These should help superconductor electronics make



(a)



(b)



(c)

Fig. 24. Transient digitizer instrument. (a) Block diagram. (b) A superconductor IC chip containing two 6-b transient digitizers based on flash ADCs. (c) Fast pulse captured by the transient digitizer (solid line) is superimposed on a sampling oscilloscope measurement of the same waveform (points). With a 32-stage shift register, the acquisition time was 4 ns for 8 GSample/s (left) and 2 ns for 16 GSample/s (right) [4].

the transition from specialized laboratory instrumentation to commercial markets.

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REFERENCES

[1] T. Van Duzer and C. W. Turner, *Principles of Superconducting Devices and Circuits*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1999.

[2] K. K. Likharev, *Dynamics of Josephson Junctions and Circuits*. New York: Gordon & Breach, 1986.

[3] A. M. Kadin, *Introduction to Superconducting Circuits*. New York: Wiley, 1999.

[4] S. B. Kaplan, P. D. Bradley, D. K. Brock, D. Gaidarenko, D. Gupta, W.-Q. Li, and S. V. Rylov, "A superconductor flash digitizer with on-chip memory," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3020–3025, June 1999.

[5] O. A. Mukhanov, V. K. Semenov, W. Li, T. V. Filippov, D. Gupta, A. M. Kadin, D. K. Brock, A. F. Kirichenko, Y. A. Polyakov, and I. V. Vernik, "A superconductive high-resolution ADC," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 601–606, Mar. 2001.

[6] A. M. Kadin and O. A. Mukhanov, "Analog-to-digital converters," in *Handbook of Superconducting Materials*, D. Cardwell and D. Ginley, Eds. Bristol, UK: Inst. of Phys., 2002, pp. 1815–1824.

[7] J. X. Przybysz, "Josephson analog-to-digital converters," in *The New Superconducting Electronics*, H. Weinstock, Ed. Dordrecht, The Netherlands: Kluwer, 1992, pp. 329–361.

[8] G. S. Lee and D. A. Petersen, "Superconductor A/D converters," *Proc. IEEE*, vol. 77, pp. 1264–1273, Aug. 1989.

[9] H. Hayakawa, N. Yoshikawa, S. Yorozu, and A. Fujimaki, "Superconducting digital electronics," in *Proc. IEEE*, vol. 92, Oct. 2004, pp. 1549–1563.

[10] R. Kleiner, D. Koelle, F. Ludwig, and J. Clarke, "Superconducting quantum interference devices: State-of-the-art and applications," in *Proc. IEEE*, vol. 92, Oct. 2004, pp. 1534–1548.

[11] C. A. Hamilton, "Josephson voltage standards," *Rev. Sci. Instrum.*, vol. 71, pp. 3611–3623, Oct. 2000.

[12] V. K. Semenov, "Digital to analog conversion based on processing of SFQ pulses," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 2637–2640, Mar. 1993.

[13] K. K. Likharev and V. K. Semenov, "RSFQ logic/memory family: A new Josephson-junction technology for sub-terahertz clock-frequency digital systems," *IEEE Trans. Appl. Superconduct.*, vol. 1, pp. 3–28, Mar. 1991.

[14] P. Bunyk, K. Likharev, and D. Zinoviev, "RSFQ technology: Physics and devices," *Int. J. High Speed Electron. Syst.*, vol. 11, pp. 257–305, Mar. 2001.

[15] D. K. Brock, E. K. Track, and J. M. Rowell, "Superconductor ICs: The 100 GHz second generation," *IEEE Spectr.*, vol. 37, pp. 40–46, Dec. 2000.

[16] K. K. Likharev, O. A. Mukhanov, and V. K. Semenov, "Resistive single flux quantum logic for the Josephson-junction digital technology," in *Proc. SQUID'85*, H.-D. Hahlbohm and K. Lübbig, Eds. Berlin, Germany: W. de Gruyter, pp. 1103–1108.

[17] O. A. Mukhanov, V. K. Semenov, and K. K. Likharev, "Ultimate performance of the RSFQ logic circuits," *IEEE Trans. Magn.*, vol. MAG-23, pp. 759–762, Mar. 1987.

[18] V. P. Koshelets, K. K. Likharev, V. V. Migulin, O. A. Mukhanov, G. A. Ovsyannikov, V. K. Semenov, I. L. Serpuchenko, and A. N. Vystavkin, "Experimental realization of a resistive single flux quantum logic circuit," *IEEE Trans. Magn.*, vol. MAG-23, pp. 755–758, Mar. 1987.

[19] D. K. Brock, "RSFQ technology: Circuits and systems," *Int. J. High Speed Electron. Syst.*, vol. 11, pp. 307–362, Mar. 2001.

[20] W. Chen, A. V. Rylyakov, V. Patel, J. E. Lukens, and K. K. Likharev, "Rapid single flux quantum T-flip-flop operating up to 770 GHz," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3212–3215, June 1999.

[21] A. F. Kirichenko, S. Sarwana, D. Gupta, I. Rochwarger, and O. A. Mukhanov, "Multi-channel time digitizing system," *IEEE Trans. Applied Supercond.*, vol. 13, pp. 454–458, June 2003.

[22] A. M. Kadin, C. A. Mancini, M. J. Feldman, and D. K. Brock, "Can RSFQ logic circuits be scaled to deep submicron dimensions?," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 1050–1055, Mar. 2001.

[23] The International Technology Roadmap for Semiconductors (2004). [Online]. Available: http://public.itrs.net

[24] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta–Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE, 1997.

[25] R. H. Walden, "Analog-to-digital converter survey and analysis," *IEEE J. Select. Areas Commun.*, vol. 17, pp. 539–550, Apr. 1999.

[26] L. Abelson and G. Kerber, "Superconductor integrated circuit fabrication technologies," in *Proc. IEEE*, vol. 92, Oct. 2004, pp. 1517–1533.

[27] D. Gupta, A. M. Kadin, R. J. Webber, I. Rochwarger, D. Bryce, W. J. Hollander, Y. U. Kim, R. P. Kraft, J. W. Kim, and J. F. McDonald, "Integration of cryocooled superconducting ADC and SiGe output amplifier," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 477–483, June 2003.

[28] A. G. Sun, B. J. Dalrymple, D. J. Durand, M. W. Johnson, J. A. Luine, and A. Spooner, "10 K NbN DSP module for IR sensor applications," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 312–317, Mar. 2001.

[29] M. G. Forrester, B. D. Hunt, D. L. Miller, J. Talvacchio, and R. M. Young, "Analog demonstration of a high-temperature superconducting sigma–delta modulator with 27 GHz sampling," *Supercond. Sci. Technol.*, vol. 12, pp. 698–670, Nov. 1999.

[30] B. Ruck, Y. Chong, R. Dittman, and M. Siegel, "First-order sigma–delta modulator in HTS bicrystal technology," *Physica C: Supercond.*, vol. 326–327, pp. 170–176, June 1999.

[31] A. Y. Kidiyarova-Shevchenko, D. E. Kirichenko, Z. Ivanov, F. Komissinsky, E. A. Stepancov, M. M. Khapaev, and T. Claeson, "Single-flux-quantum comparators for HTS A/D converters," *Physica C: Supercond.*, vol. 326–327, pp. 83–92, Nov. 1999.

[32] A. H. Sonnenberg, I. Oomen, H. Hilgenkamp, G. J. Gerritsma, and H. Rogalla, "Sigma–delta A/D converter in HTS ramp-edge technology," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 200–204, Mar. 2001.

[33] P. Bradley and H. Dang, "Design and testing of quasione junction SQUID-based comparators at low and high speed for superconductor flash A/D converters," *IEEE Trans. Appl. Superconduct.*, vol. 1, pp. 134–139, Sept. 1991.

[34] ——, "A 6-bit Josephson flash A/D converter with GHz input bandwidth," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 2550–2557, Mar. 1993.

[35] S. B. Kaplan, S. V. Rylov, and P. Bradley, "Real-time error correction for flash analog to digital converter," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 2822–2825, June 1997.

[36] C. J. Anderson, "Josephson look-back analog to digital converter," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 2769–2773, Mar. 1993.

[37] J. P. Hurrell, D. C. Pridmore-Brown, and A. H. Silver, "A/D conversion with unlatched SQUID's," *IEEE Trans. Electron Devices*, vol. 27, pp. 1887–1896, Oct. 1980.

[38] C. A. Hamilton and F. L. Lloyd, "100 GHz binary counter based on dc SQUIDs," *IEEE Electron Device Lett.*, vol. 3, pp. 335–338, Nov. 1982.

[39] A. Iwata, N. Sakimura, M. Nagata, and T. Morie, "An architecture of delta sigma A-to-D converters using a voltage controlled oscillator as a multi-bit quantizer," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, 1998, pp. 389–392.

[40] M. W. Johnson, B. J. Dalrymple, D. J. Durand, Q. P. Herr, and A. H. Silver, "Wide bandwidth oscillator/counter A/D converter," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 607–611, Mar. 2001.

[41] O. A. Mukhanov, S. Sarwana, D. Gupta, A. F. Kirichenko, and S. V. Rylov, "Rapid single flux quantum technology for SQUID applications," *Physica C: Superconduct.*, vol. 368, pp. 196–202, Mar. 2002.

[42] S. Sarwana, D. Gupta, A. Kirichenko, T. Oku, C. Otani, H. Sato, and H. Shimizu, "High-sensitivity high-resolution dual-function signal and time digitizer," *Appl. Phys. Lett.*, vol. 80, pp. 2023–2025, Mar. 2002.

[43] F. Kuo, H. Dang, S. R. Whiteley, and M. Radparvar, "A superconducting tracking A/D converter," *IEEE J. Solid-State Circuits*, vol. 26, pp. 142–145, Feb. 1991.

[44] S. V. Rylov, "Analysis of high-performance counter-type A/D converters using RSFQ logic/memory elements," *IEEE Trans. Magn.*, vol. MAG-27, pp. 2431–2434, Mar. 1991.
[45] L. V. Fillipenko, V. K. Kaplunenko, M. I. Khabipov, V. P. Koshelets, K. K. Likharev, O. A. Mukhanov, S. V. Rylov, V. K. Semenov, and A. N. Vystavkin, "Experimental implementation of analog-to-digital converter based on the reversible ripple counter," *IEEE Trans. Magn.*, vol. MAG-27, pp. 2464–2467, Mar. 1991.
[46] S. V. Rylov and R. P. Robertazzi, "Superconductive high-resolution A/D converter with phase modulation and multi-channel timing arbitration," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2260–2263, June 1995.
[47] S. R. Rylov, L. A. Bunz, D. V. Gaidarenko, M. A. Fisher, R. P. Robertazzi, and O. A. Mukhanov, "High resolution ADC system," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 2649–2652, June 1997.
[48] S. V. Rylov, D. K. Brock, D. V. Gaidarenko, A. F. Kirichenko, J. M. Vogt, and V. K. Semenov, "High resolution ADC using phase modulation-demodulation architecture," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3016–3019, June 1999.
[49] O. A. Mukhanov, V. K. Semenov, D. K. Brock, A. F. Kirichenko, W. Li, S. V. Rylov, J. M. Vogt, T. V. Filippov, and Y. A. Polyakov, "Progress in the development of a superconductive high-resolution ADC," in *Extended Abstracts ISEC'99*, Berkeley, CA, pp. 13–16.
[50] O. A. Mukhanov, V. K. Semenov, I. V. Vernik, A. M. Kadin, T. V. Filippov, D. K. Brock, I. Rochwarger, and Y. A. Polyakov, "High-resolution ADC operation up to 19.6 GHz clock frequency," *Supercond. Sci. Technol.*, vol. 14, pp. 1065–1070, Dec. 2001.
[51] J. C. Lin, V. K. Semenov, and K. K. Likharev, "Design of SFQ-counting analog-to-digital converter," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2252–2259, June 1995.
[52] V. K. Semenov, Y. A. Polyakov, and D. Schneider, "Implementation of oversampling analog-to-digital converter based on RSFQ logic," in *Extended Abstracts ISEC'97*, Berlin, Germany, pp. 41–43.
[53] V. K. Semenov, Y. A. Polyakov, and T. V. Filippov, "Superconducting delta ADC with on-chip decimation filter," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3026–3029, June 1999.
[54] V. K. Semenov and M. A. Voronova, "DC voltage multipliers: A novel application of synchronization in Josephson junction arrays," *IEEE Trans. Magn.*, vol. 25, pp. 1432–1435, Mar. 1989.
[55] V. K. Semenov and Y. A. Polyakov, "Circuit improvements for a voltage multiplier," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 550–553, Mar. 2001.
[56] J. X. Przybysz, D. L. Miller, E. H. Naviasky, and J. H. Kang, "Josephson sigma–delta modulator for high dynamic range A/D conversion," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 2732–2735, Mar. 1993.
[57] P. H. Xiao and T. Van Duzer, "Superconducting delta–sigma oversampling A/D converter," *IEEE Trans. Appl. Superconduct.*, vol. 3, pp. 2625–2628, Mar. 1993.
[58] D. L. Miller, J. X. Przybysz, D. L. Meier, J. H. Kang, and A. H. Worsham, "Characterization of sigma–delta analog to digital converter," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2453–2456, June 1995.
[59] A. Fujimaki, K. Nakazono, H. Hawegawa, T. Sato, A. Akahori, N. Takeuchi, F. Furuta, M. Katayama, and H. Hayakawa, "Broad-band software-defined radio receivers based on superconductor devices," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 318–321, Mar. 2001.
[60] J. X. Przybysz, D. L. Miller, and E. H. Naviasky, "Two-loop modulator for sigma–delta analog to digital converter," *IEEE Trans. Appl. Superconduct.*, vol. 5, pp. 2248–2251, June 1995.
[61] D. L. Miller, J. X. Przybysz, A. H. Worsham, and E. J. Dean, "Flux quantum sigma–delta analog-to-digital converters for rf signals," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 4026–4029, June 1999.
[62] A. H. Worsham, D. L. Miller, P. D. Dresselhaus, A. H. Miklich, and J. X. Przybysz, "Superconducting modulators for high-dynamic range delta–sigma analog-to-digital converters," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3157–3160, June 1999.
[63] S. Hirano, H. Hasegawa, S. Nagasawa, S. Kato, K. Miyahara, and Y. Enomoto, "Feedback-current-injection second-order lowpass sigma–delta modulator," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 488–491, June 2003.
[64] S. Hirano, H. Hasegawa, S. Nagasawa, K. Miyahara, Y. Enomoto, and K. Tanabe, "Second-order lowpass sigma–delta modulator with parallel multiple-flux-quantum feedback driver," *Physica C*, vol. 392, pp. 1456–1460, Oct. 2003.
[65] J. X. Przybysz and D. L. Miller, "Bandpass sigma–delta modulator for analog-to-digital converter," U.S. Patent 5 341 136, Aug. 23, 1994.
[66] T. Hashimoto, H. Hawegawa, S. Nagasawa, H. Suzuki, K. Miyahara, and Y. Enomoto, "Noise-shaping characteristics of superconducting band-pass sigma–delta modulators," *Jpn. J. Appl. Phys.*, vol. 40, pp. L1032–L1034, Oct. 2001.
[67] J. F. Bulzacchelli, H. S. Lee, J. A. Misewich, and M. B. Ketchen, "Superconducting bandpass delta–sigma modulator," *Supercond. Sci. Technol.*, vol. 12, pp. 695–697, Nov. 1999.
[68] ——, "Experimental demonstration of superconducting bandpass delta–sigma modulator," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 471–476, June 2003.
[69] ——, "Superconducting bandpass delta–sigma modulator with 2.23-GHz center frequency and 42.6-GHz sampling rate," *J. Solid-State Circuits*, vol. 37, pp. 1695–1702, Dec. 2002.
[70] V. K. Semenov, "Comparison of superconductor analog-to-digital converters (theory)," in *Extended Abstracts ISEC'99*, Berkeley, CA, pp. 23–25.
[71] ——, "Superconductor modulator with very high sampling rate for analog to digital converter," U.S. Patent 6 608 581, Aug. 19, 2003.
[72] D. Gupta and M. Radparvar, "Subranging digital SQUID ammeter," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 1261–1264, Mar. 2001.
[73] J. F. Bulzacchelli, "Superconducting Bandpass Delta–Sigma Modulator for Direct Analog-To-Digital Conversion of Microwave Radio," Ph.D. dissertation, Elect. Eng. Comput. Sci. Dept., Massachusetts Inst. Technol., Cambridge, 2003.
[74] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. ASSP-29, pp. 155–162, Apr. 1981.
[75] T. V. Filippov, S. V. Pflyuk, V. K. Semenov, and E. B. Wikborg, "Encoders and decimation filters for superconductor oversampling ADCs," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 545–549, Mar. 2001.
[76] V. K. Semenov, Y. A. Polyakov, and A. Ryzhikh, "Decimation filters based on RSFQ logic/memory cells," in *Extended Abstracts ISEC'97*, Berlin, Germany, pp. 344–346.
[77] H. Hasegawa, T. Hashimoto, S. Nagasawa, H. Suzuki, K. Miyahara, and Y. Enomoto, "Design of superconducting single flux quantum decimation filters," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 517–520, Mar. 2001.
[78] A. Sekiya, M. Tanaka, A. Akahori, A. Fujimaki, and H. Hayakawa, "Demonstration of decimation filter and high-speed testing of a component of the filter," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 579–582, June 2003.
[79] A. F. Kirichenko, O. A. Mukhanov, and A. I. Ryzhikh, "Advanced on-chip test technology for RSFQ circuits," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 3438–3441, June 1997.
[80] V. Kaplunenko, V. Borzenets, N. Dubash, and T. Van Duzer, "Superconducting single flux quantum 20 Gb/s clock recovery circuit," *Appl. Phys. Lett.*, vol. 71, pp. 128–130, July 1997.
[81] D. Gupta and Y. Zhang, "On-chip clock technology for ultra-fast digital superconducting electronics," *Appl. Phys. Lett.*, vol. 76, no. 25, pp. 3819–3821, June 2000.
[82] I. V. Vernik and D. Gupta, "Two-phase 50 GHz on-chip long Josephson junction clock source," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 587–590, June 2003.
[83] J. L. Habif, C. A. Mancini, and M. F. Bocko, "Measurement of jitter in a long Josephson junction soliton oscillator clock source," *IEEE Trans. Appl. Superconduct.*, vol. 11, pp. 1086–1089, Mar. 2001.
[84] C. A. Mancini and M. F. Bocko, "Short-term frequency stability of clock generators for multigigahertz rapid-single-flux quantum digital circuits," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 25–37, Mar. 2003.
[85] D. Brock and M. Pambianchi, "A 50 GHz monolithic RSFQ digital phase-locked loop," in *IEEE Int. Microwave Symp. Dig.*, vol. 1, 2000, pp. 353–356.
[86] A. K. Salkintzis, H. Nie, and P. T. Mathiopoulos, "ADC and DSP challenges in the development of software radio base stations," *IEEE Pers. Commun.*, vol. 6, pp. 47–55, Aug. 1999.
[87] J. Mitola, *Software Radio Architecture*. New York: Wiley, 2000.
[88] E. B. Wikborg, V. K. Semenov, and K. K. Likharev, "RSFQ front-end for a software radio receiver," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3615–3618, June 1999.
[89] D. K. Brock, O. A. Mukhanov, and J. Rosa, "Superconductor digital rf development for software radio," *IEEE Commun. Mag.*, vol. 39, pp. 174–179, Feb. 2001.

[90] O. Mukhanov, D. Gupta, A. Kadin, J. Rosa, V. Semenov, and T. Filippov, "Superconductive digital-RF transceiver components," in *Proc. SDR Technical Conf.*, vol. 1, San Diego, CA, 2002, pp. 227–232.
[91] D. Gupta, O. Mukhanov, A. Kadin, J. Rosa, and D. Nicholson, "Benefits of superconductive Digital-RF transceiver technology to future wireless systems," in *Proc. SDR Technical Conf.*, vol. 1, San Diego, CA, 2002, pp. 221–226.
[92] M. Maezawa, M. Suzuki, H. Sasaki, and A. Shoji, "Analog-to-digital converter based on RSFQ technology for radio astronomy applications," in *Extended Abstracts ISEC'01*, Osaka, Japan, 2001, pp. 451–452.
[93] J. Kang, D. Gupta, and S. B. Kaplan, "Demonstration of RSFQ digitizer on a multi-chip module," *IEEE Trans. Appl. Superconduct.*, vol. 13, pp. 1848–1851, Sept. 2002.
[94] Q. P. Herr, A. D. Smith, and M. S. Wire, "High-speed data link between digital superconducting chips," *Appl. Phys. Lett.*, vol. 80, pp. 3210–3212, Apr. 2002.
[95] D. Gupta, D. Gaidarenko, and S. V. Rylov, "A 16-bit serial analog-to-digital converter module with optical output," *IEEE Trans. Applied Supercond.*, vol. 9, pp. 3030–3033, June 1999.
[96] O. A. Mukhanov, A. F. Kirichenko, J. M. Vogt, and M. S. Pambianchi, "A superconductive multi-hit time digitizer," *IEEE Trans. Applied Supercond.*, vol. 9, pp. 3619–3622, June 1999.
[97] S. Pagano, V. Palmieri, A. Esposito, O. Mukhanov, and S. Rylov, "First realization of a tracking detector for high energy physics experiments based on Josephson digital readout circuitry," *IEEE Trans. Appl. Superconduct.*, vol. 9, pp. 3628–3631, June 1999.
[98] M. Radparvar and S. Rylov, "High-sensitivity digital SQUID magnetometer," *IEEE Trans. Appl. Superconduct.*, vol. 7, pp. 3682–3685, June 1997.
[99] V. K. Semenov and Y. A. Polyakov, "Fully integrated digital SQUID," in *Extended Abstracts ISEC'97*, Berlin, Germany, pp. 329–331.
[100] F. H. Uhlmann, S. Lange, M. Khabipov, and H.-G. Meyer, "Investigation of the design of a digital SQUID sensor," *Physica C*, vol. 326, pp. 72–78, Nov. 1999.

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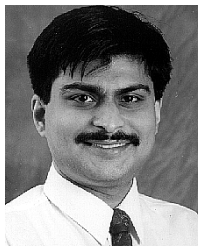

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